# “Nikola Tesla's” Approach to Prime Numbers

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**Abstract** In this paper, a piece of advice from Nikola Tesla is going to be used, in order to create a digital electronic circuit that detects/generates prime numbers. Consequently, a formula for the *n*-th prime is going to be presented.

## 1 Introduction

A piece of advice widely attributed to Nikola Tesla, that if someone wants to find secrets of the universe, she/he should think in the terms of frequency, vibration and energy [1], is going to be accepted. Here, an idea that prime numbers are related to rectangular waves of the certain periods (frequencies), is explored (prime numbers are building blocks of the system of natural numbers and our understanding of the universe mainly comes from formulas and numbers.). By doing that, it is going to be shown that a digital electronic circuit that generates/detects prime numbers can be designed. Consequently, it is possible to construct a formula for the *n*-th prime number.

## 2 Generating/detecting primes using digital electronic circuit

In this section a digital electronic circuit that can be used for detection (generation) of prime numbers is going to be presented. The key component is NT (Nikola Tesla) type Counter/Timer component. This component contains one main counter/timer part and one auxiliary counter part. The Counter/Timer has three inputs CLK, $\overline{C}$/T, Cx and one output OUT. Input CLK receives clock signal from some outer pulse generator and provides the clock to the main counter/timer. The $\overline{C}$/T input defines mode of the operation of the main counter/timer part – during the first period of input clock and as long as the value on that input is low (zero), the part works as a forward counter (initial value of the counter is zero). That input is internally held low (0) during the first period of the clock. After the first rising edge on that input (and after the first period of input clock) the counter/timer part starts to work as a timer, where the length of the interval is defined by the value of the main counter in the moment when the change of function has happened. After that moment, functioning mode of the

Counter/Timer cannot be changed without reset of electronics.

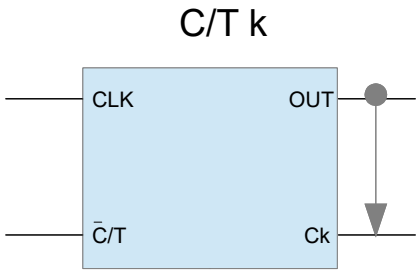


Fig. 1. Counter/Timer – NT type

Figure 1 depicts a Counter/Timer component. As long as the $\overline{C}$/T functions is a counter, value of the OUT output of the main counter/timer is high (logical 1). When the component changes the function to timer mode, OUT goes to low (logical 0) for one cycle of input clock (one that is connected to CLK input), and then jumps to high (logical 1) for *x* cycles, where *x* is a value of the internal counter in the moment of the change of functioning mode and repeats that pattern for the rest of the time. The input, marked as Cx, receives a clock from the output OUT of the Counter/Timer and represents input to auxiliary counter that keeps track of how many cycles of the main timer has been completed – its value is updated on every falling edge. Since this is important only for the analysis of the composite numbers, it won't be further discussed in this paper.

At the following figure the component C/T 1 is depicted – the Counter/Timer component that generates signal **1**. That signal is going to be used to detect the first prime – number 2. The signal **0** is the signal that has value 0 all the time. This figure, and all subsequent figures, depicts a very simplified electronic circuit that contains only the elements that are necessary for understanding the underlying principles important for this paper. Many parts that are necessary for proper functioning of those circuit are missing (e.g. power supply, clock generator, passive components like capacitors and resistors, switches and so on). Anyway, proposed electronic circuit is used to explain the principle that is used – a real implementation would be much more efficient and easier using microprocessors, but this is beyond the scope of this paper.

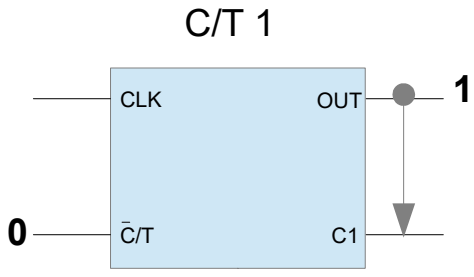


Fig. 2. Counter/Timer 1– This component gives output 1 (high) in every moment.

The following figures depict the detection circuits for primes 2, 3, 5 and 7, and corresponding signals **2**, **3**, **5** and **7**.

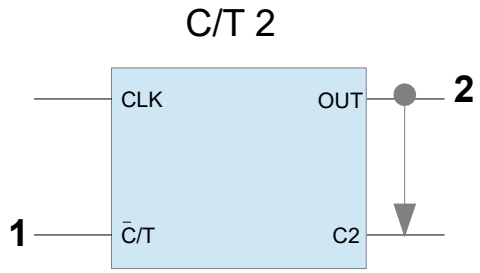


Fig. 3. Counter/Timer 2– This component detects prime number 2 and all even numbers.

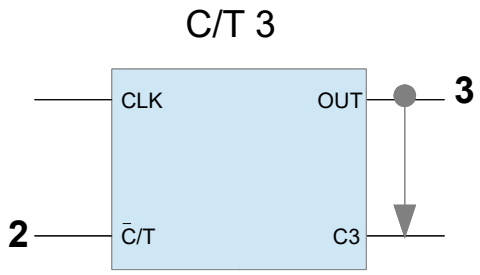


Fig. 4. Counter/Timer 3– This component detects prime number 3 and all numbers divisible by 3.

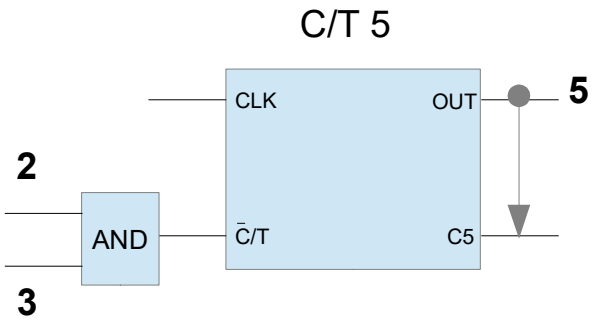


Fig. 5. Counter/Timer 5– This component detects prime number 5 and all numbers divisible by 5.

The AND box on the Fig. 5 represents standard AND logic circuit (the output is high (logical 1) only in the case when the both inputs are high (logical 1) and output is low (logical 0) for all other combinations of the inputs).

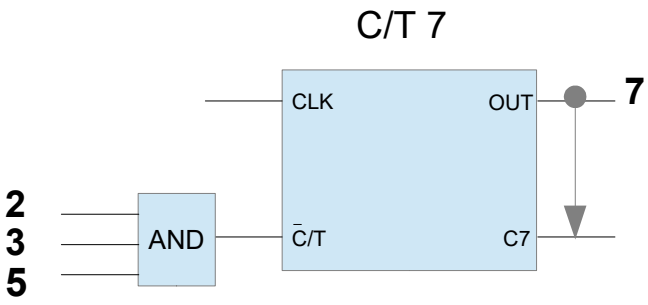


Fig. 6. Counter/Timer 7– This component detects prime number 7 and all numbers divisible by 7.

Figures 3-6 could be assembled in a single figure, but it would create more complex digital circuit that would be more complicated to follow for the people that are not familiar with electronics.

Signals **0**, **1**, **2**, **3**, **5** and **7** are depicted in the following figure.

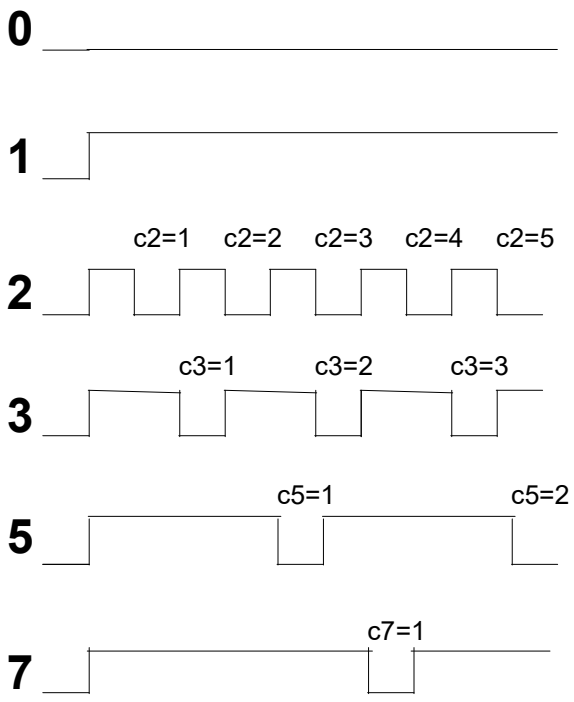


Fig. 7. Signals **0**, **1**, **2**, **3**, **5** and **7**.

A circuit for detection (generation) of the *n*-th prime Pn and corresponding signal **Pn**, is depicted in the following figure.

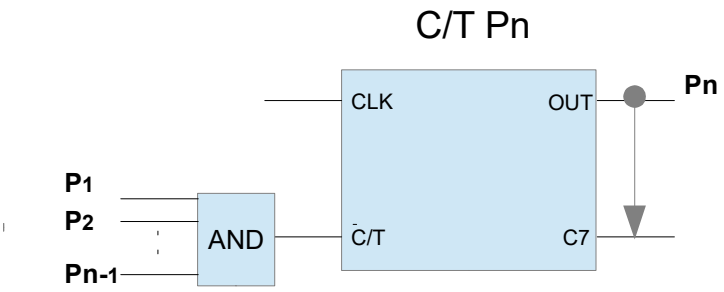


Fig. 8. Counter/Timer Pn– This component detects *n*-th prime number Pn and all numbers divisible by Pn.

It can be noticed that detection (generation) of the *n*-th prime requires that all *n* -1 primes before it to be detected. This is a naive approach and can be optimized, but it is beyond the scope of this paper. Generally, it can be concluded that process for prime number generation has recursive nature. Having in mind that a digital electronic circuit was used for the realization of a process that can generate/detect prime numbers, it is easy to conclude that it must be possible to construct a formula for the *n*-th prime number. One possible choice is a formula for the *n*-th prime number $P_n$ given by the following equation:

$$P_n = \min_k \left( \left( \prod_{i=1}^{n-1} mod\left(k, P_i\right) \right) > 0 \right), k \in N, k > P_{n-1}. \qquad (1)$$

So, the formula (1) can be used for recursive generation of all prime numbers. As it was previously mentioned, this is a naive approach (in the sense that all *n* - 1 prime numbers should participate in generation of the *n*-th prime number – *i*-th prime number should participate only when $k \geq P_i^2$ ) that can be optimized, but it is not going to be discussed here. It is obvious that proposed formula is not "perfect" for calculation of quintillionth prime number, but it can be used for some mathematical proofs.

## 3 One problem in which the proposed approach could be useful

Using formula (1) it is not difficult to prove the following Theorem (a proof is not going to be presented here):

**Theorem 1:** The first $n$ prime numbers $p_1, p_2, \ldots, p_n$ cannot create a sequence of consecutive composite numbers, such that every composite number in the sequence has as the smallest divisor one of those prime numbers, that is longer than

$$2p_{n-1} - 1.$$

In general case (especially for big $n$), it also can be concluded that such a sequence can be created only in the case when the numbers in the sequence are much bigger than $p_{n-1}^2$.

## 4 Conclusion

In this paper it has been shown that prime numbers are deterministic numbers that could be obtained through a simple minimization process that is recursive in its nature. It has been shown that it is possible to create a digital electronic circuit that detect/generate prime numbers. The proposed formula for the $n$-th prime number can be useful in solving some problems, and one such problem has been presented. Using the proposed idea it is possible to create a rectangular waves that are related to rational numbers and possibly understand why $\pi$ is frequently present in the sums of the infinite number of reciprocal natural numbers.

## References:

1. https://en.m.wikiquote.org/wiki/Nikola_Tesla. (Author was not able to find the reference to the quote, widely attributed to Nikola Tesla, that is used as a starting point of the research presented in this paper.)