FinFET Chronicles: Navigating the Silicon Horizon in the Era of Nanoarchitecture

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***Abstract*—This paper investigates FinFET transistor technology, aiming to address limitations in conventional planar CMOS transistors. The motivation stems from the escalating demand for high-performance, low-power devices in sub-10nm technology nodes. The challenges of short-channel effects, leakage currents, and scalability constraints in planar CMOS transistors have prompted exploration into novel architectures like FinFETs. This research provides an indepth analysis of FinFETs' three-dimensional structure, fabrication, materials, and design considerations. We evaluate their advantages and limitations compared to traditional transistors in terms of power consumption, speed, and scalability. Our approach involves comparative studies utilizing simulations, material analysis, and empirical data. By merging theory with practical insights, this paper aims to offer a comprehensive view of FinFET technology's potential and challenges in modern semiconductor applications. In conclusion, this study sheds light on FinFET transistors, emphasizing their fabrication, design, and performance characteristics. It highlights their promise as a solution to semiconductor industry challenges, paving the way for next-generation electronic devices.**

***Index Terms*—FinFET Technology, CMOS Multi-Gate Transistors, Solid State Devices, Three-Dimensional Transistors, Sub-10nm Technology, Short-Channel Effects, Leakage Currents, Scalability Constraints, High-Performance Electronics, Low-Power Devices, Comparative Studies, Power Consumption, Speed Evaluation, Semiconductor Fabrication, Material Analysis, Design Considerations, Empirical Data, Next-Generation Electronics, Semiconductor Industry Challenges.**

I. Introduction

The semiconductor industry has relentlessly pursued advancements in transistor technology to propel electronic devices into new realms of efficiency and performance. Conventional planar CMOS transistors have been instrumental in driving these advancements, yet their limitations have become increasingly evident, especially when scaling down to sub-10nm technology nodes. Issues such as short-channel effects, escalating leakage currents, and challenges in maintaining scalability have underscored the necessity for exploring alternative transistor architectures. In response to these limitations, FinFET (Fin Field-Effect Transistor) technology has emerged as a focal point of innovation. Distinguished by its three-dimensional fin-like structure, FinFETs offer a promising solution to circumvent the shortcomings of planar CMOS transistors. The potential of FinFETs lies in their ability to potentially achieve heightened performance, diminished power consumption, and improved scalability compared to the traditional planar transistor designs. This paper aims to comprehensively delve into FinFET transistor technology, seeking to bridge the gap in our understanding. It intends to elucidate the intricate fabrication processes, materials, design considerations, and crucial performance metrics underlying FinFETs. Through an exhaustive analysis, this research endeavor seeks to offer valuable insights into both the advantages and limitations of FinFETs when compared to their conventional transistor counterparts. The ultimate goal is to contribute significantly to the knowledge base in semiconductor technology by shedding light on the capabilities and drawbacks of FinFET technology. The primary research question steering this investigation is: "What are the fundamental characteristics and performance attributes of FinFET transistors, and how do they compare to traditional planar CMOS transistors?" This guiding question will shape the examination of the structure, fabrication methods, materials, and performance metrics of FinFETs within the context of addressing the limitations prevalent in existing transistor technology.

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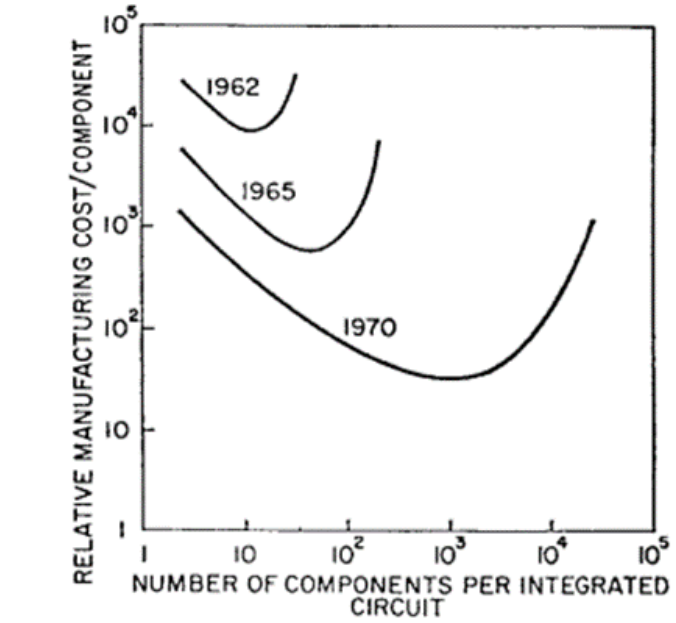
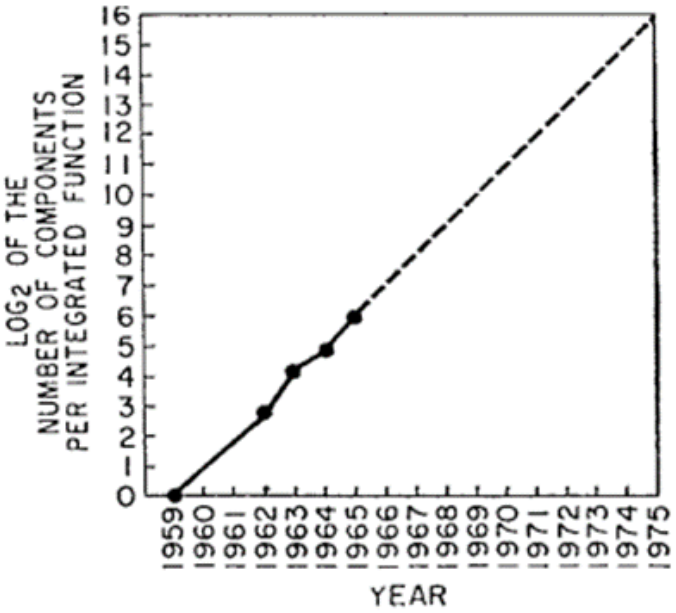
II. Preliminaries

A. Historical background

A metal-oxide-semiconductor (MOS) device with the gate positioned on both sides of a thin vertical semiconductor body resting on a substrate is known as a FinFET, or "fin" field-effect transistor (FET). It was Yutaka Hayashi who created this innovative apparatus at the manufacturing device technology was established in the late 1990s by the research group headed by Chenming Hu at the University of California Microfabrication Lab, Berkeley, CA [14], and the Electrotechnical Laboratory, Tsukaba, Japan in 1980 [13]. An ultrathin body "fin" made of a semiconductor material, such silicon, serving as a FET device's channel is what the acronym FinFET refers to. For better device performance in FinFET device architecture, the gate can be positioned on two, three, four, or all four sides of the ultrathin-body fin. This Also followed the trend that was observed by G.E Moore (Moore's law) as he predicted the the shrinking the of electronic components in integerated circuits and the reductions of its cost every year.



(a) Over Costs



(b) Over Years

Fig. 1: Moore's Law

The excerpt [15] encapsulates Gordon Moore's seminal 1965 publication, heralding the transformative potential of integrated electronics. Moore's insights laid the groundwork for "Moore's Law," a prophetic projection outlining the exponential evolution of integrated circuits. He anticipated their capacity to accommodate an increasing number of components while simultaneously reducing production costs. Moore envisioned a future where integrated circuits would revolutionize technology across multiple domains, foreseeing their pervasive presence in home computing, portable communication devices, and complex systems like telecommunications. His predictions proved prescient, as these innovations became commonplace. The text underscores the pivotal role of integrated electronics in diverse spheres, particularly in military applications and commercial computing. Its attributes, such as heightened reliability, compactness, and improved performance, rendered systems employing integrated electronics highly advantageous. Furthermore, the passage highlights the ongoing evolution and amalgamation of diverse microelectronic techniques, emphasizing the potential for synergistic advancements through the integration of varied approaches. Moore's foresight profoundly influenced the trajectory of technology, substantiating the pervasive integration of electronics in modern life. His anticipations continue to shape technological progress, validating the fundamental role played by integrated electronics in contemporary society.

B. Theoretical background

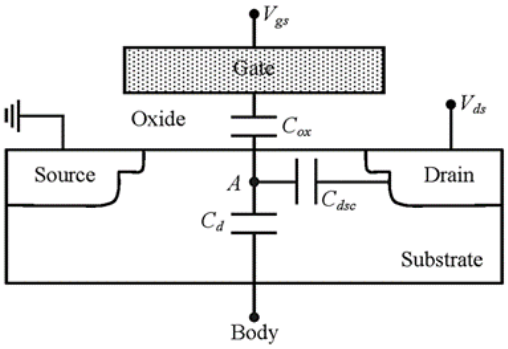


Fig. 2: Gate Capacitance

A conventional MOSFET device showing gate capacitance C_{ox}, bulk capacitance C_d, and the source-drain to channel coupling capacitances Cdsc; with scaling L_g, C_d increases due to the increase in C_{dsc} and controls the channel potential in the nanometer node devices; here, A represents the capacitance voltage divider node between Cox and the effective capacitance of C_d and C_{dsc}. the possibilities of the waterway. The effective value of C_d rises as L_g falls, and V_{gs} no longer has complete control over the channel. In extreme circumstances, V_{ds} alone can switch on the transistor and V_{gs} have less control than V_{ds}.

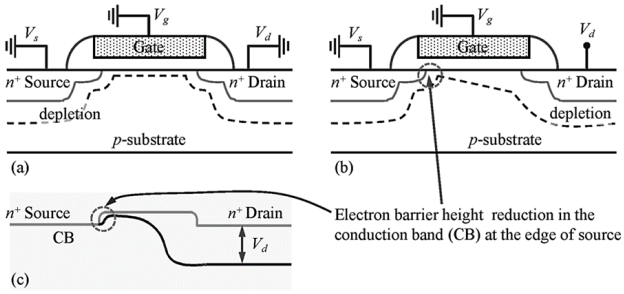


Fig. 3: Electron Barrier

for a MOSFET device with a size of 30 nm. We see the continuously declining subthreshold device performance with

lowering L_ga from 250 nm and below, before the extreme case $L_g = 30nm$ is attained. By decreasing the value of T_{ox} proportionate to L_g, one can maximize C_g, which is the optimal MOSFET scaling rule to increase the gate control of the channel [16]. But beyond the 20 nm domain, the traditional scaling method can only enhance V_{gs} control of the MOSFET channel and leakage current. due to fundamental physical constraints, as demonstrated by the two-dimensional (2D) cross-section of a perfect planar MOSFET [17], even with the lowest feasible T_{ox}. Since the leakage paths further from the gate are only weakly regulated by V_{gs}, it is evident that they are worse than the surface leakage path. As a result, V_{ds} through the huge C_{dsc} in a small Lg device can quickly lower the potential barriers along these weakly controlled routes.

C. Thin-Body field-effect TransisTors

The novel device architecture to ensure greater gate control of the channel for FET devices are to use thin-body silicon as the channel. There are two ways to enhance the gate control of the body and reduce the drain control of the channel and C_{dsc} by (1) ultrathin body on an SOI substrate and (2) multiple gates around an ultrathin-body silicon channel [16].

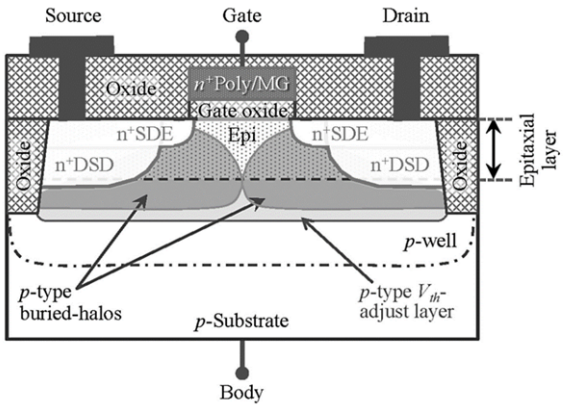


Fig. 4: Thin Body

D. Single-Gate Ultrathin-Body Field-Effect Transistors

The SCEs in a MOSFET can be significantly suppressed by using an ultrathin SOI substrate [18] to bring silicon closer t the gate. However, the improvement of SCEs in MOSFET on SOI substrates depends on the technology parameters suc as silicon film thickness t_{si} , gate-dielectric (silicon dioxide thickness, and body doping concentration. The reported dat show that the leakage current decreases with a decrease c t_{si} . And, by reducing t_{si} [19] [20] to only around 7 to 1 nm, SCEs can be significantly suppressed by eliminating th worst leakage paths terminated in the buried silicon dioxide [19] [20].

III. STRUCTURE

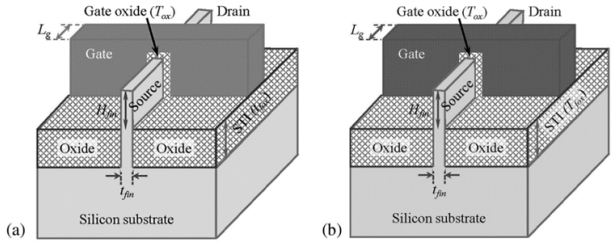


Fig. 5: FinFET Structured [21]

The structure of an ideal DG-FinFET on a bulk-silicon substrate comprises a three-dimensional arrangement (a) and a two-dimensional cross-section (b) along the cutline XX'. To operate as a DG-FinFET with sidewall gates, a thick masking oxide of thickness T_{mask} is used. This device is characterized by parameters like gate or channel length L_g, fin height H_{fin}, fin thickness or width t_{fin}, gate oxide thickness T_{ox}, body doping N_b, and source-drain junction X_j. Shallow trench isolation (STI) with field oxide thickness T_{fox} is employed for device isolation on the same substrate. Visualizing the DG-FinFET structure akin to a DG-MOSFET, we focus on the active transistor region along the x-axis and up to H_{fin} along the z-axis from the 2D-FinFET cross-section (b) to obtain the structure in (a). Rotating this structure by 90 degrees to the right around the y-axis brings the left sidewall gate on top and the right sidewall gate at the bottom, defining the zx-plane in (b). Further rotation by 90 degrees to the left around the x-axis yields the DG-MOSFET structure in (c), representing the yx-plane. The current in a FinFET flows through the entire surface of each fin height H_{fin} under the gate-stack from the respective sidewall gate. For a DG-FinFET, the width (W) is $2H_{fin}$, while for a triple-gate FinFET, it includes the top gate contribution as $W = 2H_{fin} + t_{fin}$. Despite the top gate impacting the effective width and current drive, the mathematical formulation of DG-MOSFET applies to triple-gate FinFETs by considering the device width appropriately. In reality, properly designed FinFETs with target values of channel length L and fin thickness t_{fin} exhibit immunity to short-channel effects (SCE) if $t_{fin} \ll L$. This scaling relation between t_{fin} and L aligns with semiconductor physics principles, suppressing SCEs in FinFETs.

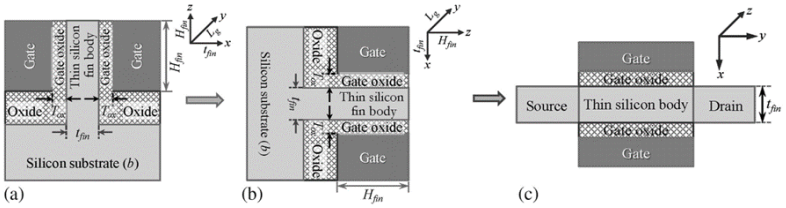


Fig. 6: Multi Plan Views for FinFET

IV. Basic idea of operation

The FinFET transistor is superior to traditional planar transistors in various ways, which improves digital switching. These benefits include decreased power consumption, shorter switching times, improved performance, scalability, less power leakage, increased current density, and improved electrostatic channel management. With its thin vertical fin and gate completely encircling the channel on three sides, the FinFET's unusual three-dimensional architecture enhances channel control, resulting in better short-channel behaviour and lower leakage power. Because of the consequent ability to achieve greater drive currents, lower operating voltages, and a considerable decrease in static leakage current,FinFETs are the preferred transistor technology for providing high-performance, power-efficient solutions in digital circuits because of this, which also makes it possible to achieve lower operating voltages, larger drive currents, and a notable decrease in static leakage current [10] [11] [12].

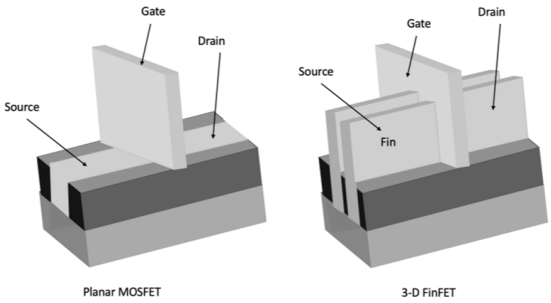
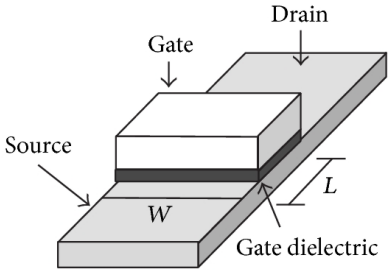
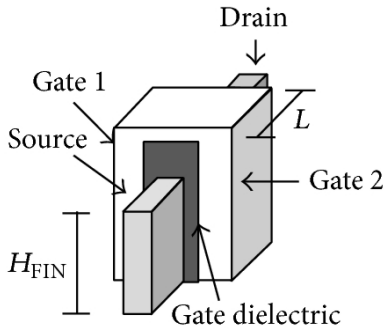


Fig. 7: MOSFET vs FinFET



(a) Planar MOSFET



(b) FinFET

Fig. 8: Structural comparison planar MOSFET and FinFET.

$$P_D = \frac{f_c \times C \times V_{dd}^2}{A} \tag{1}$$

$$I_{on} = \mu \times C_{ox} \times \frac{W}{L} \times (V_{gs} - V_{th})^2 \tag{2}$$

$$I_{off} = 100\ \frac{W}{L} \times e^{\frac{-V_t}{n}\phi_t} \tag{3}$$

$$n = 1\ +\ \frac{C_d}{C_{ox}} \tag{4}$$

A FinFET is a type of field-effect transistor (FET) that is not entirely planar, but rather features a thin vertical fin. To provide a totally depleted operation, the gate is completely "wrapped" around the channel produced between the source and the drain on three sides. As a result, chips could operate with less voltage and leakage Current (Lower Power consumption). A FinFET's body is made of a thin silicon film that is wrapped over the conducting channel, similar to how a traditional MOSFET works. The structure looks like a set of fins when seen is where the term came from. Compared to traditional MOSFET technology, FinFET devices have better short-channel behaviour, much shorter switching times, and greater current densities. It is the basis for modern nanoelectronic semiconductor device fabrication and became the dominant gate design at 14 nm, 10 nm, and 7 nm process nodes [7] [5] [8] [9].

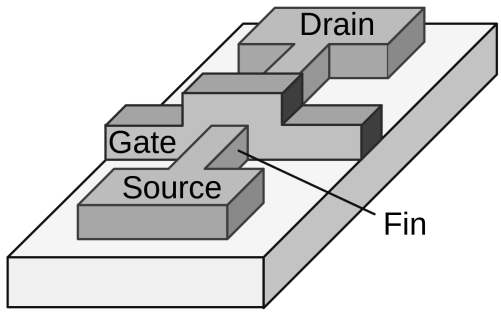


Fig. 9: Doublegate FinFET

V. Characteristics

FinFET devices are characterized by a three-dimensional configuration, utilizing vertical fins that protrude from the silicon substrate. This innovative design provides improved control over the flow of current, overcoming issues associated with leakage current and power consumption in conventional planar transistors. The fin structure allows for a more efficient use of space and enables the continued miniaturization of semiconductor components, a crucial aspect in the pursuit of higher transistor density on a chip. The core features of a FinFET device include a gate or channel length L_g, fin height H_{fin}, fin thickness or width t_{fin} , and a thick masking oxide used for electrical operation. The device operates as a Double-Gate FinFET (DG-FinFET), utilizing sidewall gates for effective control of the channel though there are some conditions for optimal control [21].

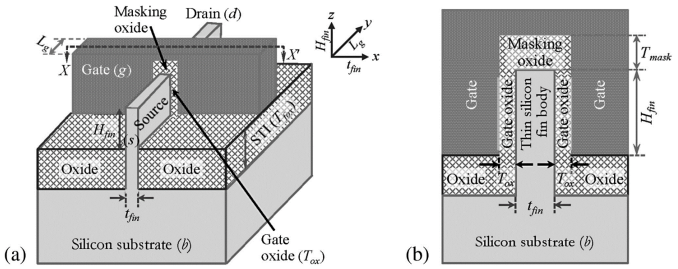


Fig. 10: FinFET Elevation

A. Depletion Region Thickness $X_{ch,g}$

To guarantee complete gate control, the fin depletion width $X_{ch,g}$ should satisfy the relation:

$$X_{ch,g} \geq \frac{t_{fin}}{2} \tag{5}$$

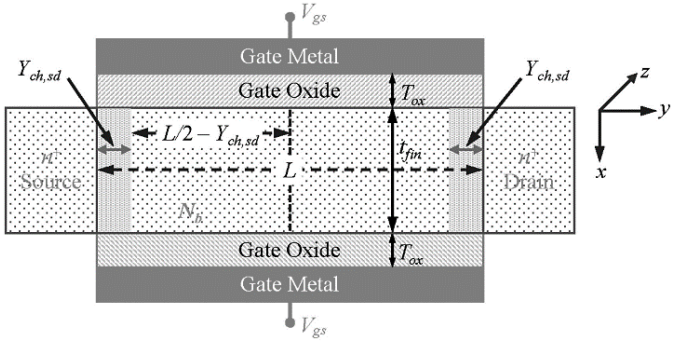


Fig. 11: FinFET Plan View

where: $X_{ch,g}$ is the thickness of the depletion region due to each gate. This condition ensures that the gate bias depletes the entire fin width.

B. Lateral Channel Depletion $Y_{ch,sd}$

To prevent source-drain punchthrough, the width of the lateral channel depletion region $Y_{ch,sd}$ due to V_{sd} at each end of the channel must be such that the neutral channel length $\frac{L}{2} - Y_{ch,sd}$ in the y-direction along the channel must satisfy:

$$\frac{L}{2} - Y_{ch,sd} \geq X_{ch,g} \tag{6}$$

ensuring that the neutral channel length in the y-direction along the channel is maintained. Using the limiting condition, $X_{ch,g} = \frac{t_{fin}}{2}$ we get:

$$\frac{L}{2} - Y_{ch,sd} > \frac{t_{fin}}{2} \tag{7}$$

We can express the depletion width in the silicon $Y_{ch,sd}$ in terms of the equivalent dielectric thickness of the gate as follows:

$$Y_{ch,sd} = \frac{K_{si}}{K_{ox}}\ T_{ox} \tag{8}$$

where K_{si} is the dielectric constant of silicon fin, K_{ox} is the dielectric constant of gate oxide and T_{ox} is the gate oxide thickness.

Therefore, after rearranging the previous equation, we get that the scaling condition for optimal gate control is as follows:

$$\frac{t_{fin}}{2} + \frac{K_{si}}{K_{ox}}\ T_{ox} \ll \frac{L}{2} \tag{9}$$

Usually speaking $Y_{ch,sd} \ll \frac{t_{fin}}{2}$, therefor the condition can be simplified to:

$$\frac{t_{fin}}{2} \ll \frac{L}{2} \tag{10}$$

C. Drain Current Modeling

To effectively address diverse Multi-gate Field-Effect Transistor (FET) architectures, one proposed technique involves classifying them into two models: a common gate model and an asymmetric/independent gate model. In the common gate model, all gates within the multi-gate FET are electrically interconnected and biased at the same voltage, assuming uniform gate workfunctions and dielectric thicknesses on multiple fin sides. The asymmetric/independent gate model, in contrast, allows different workfunctions and dielectric thicknesses on the upper and lower fin surfaces and permits independent biasing of the two gates. This categorization provides a structured approach to modeling and understanding the behavior of various multi-gate FET configurations. Many compact models for multi-gate FinFETs have been developed over the years. BSIM-CMG(Berkeley Short-channel IGFET Model – Common MultiGate) and BSIM-IMG(BSIM-Independent Multi-Gate) are surface potential-based models, and their use of surface potential confers inherent advantages. Specifically, surface potential models offer a notable benefit by providing continuous and smooth expressions for terminal currents and charges across various regions of operation [6].

D. BSIM-CMG Model Results

Using parameters:

$$N_A = 3 \times 10^{18} cm^3,\ T_{si} = 20nm,\ T_{ox} = 2nm$$

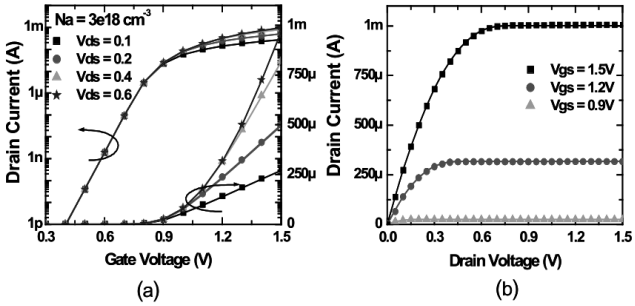


Fig. 12: BSIM-CMG Transfer and Output Characteristics [6]

VI. Practical Applications

FinFET transistors have a special use in high-performance computer systems. FinFET transistors are perfect for high-performance computer applications because they have several benefits over conventional MOSFETs, including lower power consumption, greater current density, and shorter switching

times. These components provide enhanced performance and energy efficiency in data centres, supercomputers, and other high-performance computing systems. They are utilised in sophisticated CPU cores, memory controllers, and high-speed interfaces. []FinFET transistors may be utilised to build logic gates and circuits that are more dependable and efficient in high-performance computer systems. FinFET technology, for example, may be used in the design of high-performance memory controllers to provide faster access times and lower power consumption. To further improve system performance, FinFET-based interfaces may be utilised to provide high-speed, low-latency communication channels between memory, accelerators, and CPU cores. There are several advantages of using FinFET transistors in high-performance computer systems:

1) **Lower power consumption:** FinFET transistors have a lower static power consumption due to their reduced short-channel effects, which helps to conserve energy in high-performance computing systems.
2) **Higher current density:** FinFET transistors can achieve a higher current density, which allows for faster and more reliable operation in high-performance computing systems.
3) **Reduced switching times:** FinFET transistors have lower switching times compared to conventional MOSFETs, enabling faster and more responsive operation in high-performance computing systems.
4) **Improved reliability:** FinFET transistors exhibit better electrostatic control of the channel, which can lead to improved reliability and longevity in high-performance computing systems.

In summary, FinFET transistors have the potential to revolutionize high-performance computing systems by offering significant improvements in performance, energy efficiency, and reliability. Their unique advantages make them an ideal choice for advanced processor cores, memory controllers, and high-speed interfaces in high-performance computing systems [5] [7].

A. Design of Logic Gates

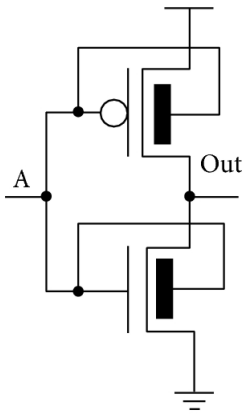


Fig. 13: FinFET Logic Gates: inverter [2]

In the realm of semiconductor technology, the design of logic gates stands as a pivotal frontier, and the application of FinFET (Fin Field-Effect Transistor) represents a groundbreaking leap forward. FinFET technology, characterized by its three-dimensional transistor structure, has redefined the landscape of electronic design [2].

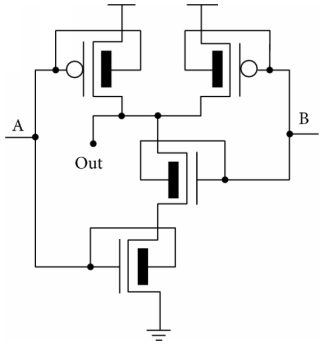


Fig. 14: FinFET Logic Gates: and [2]

B. Design of Flip-Flops

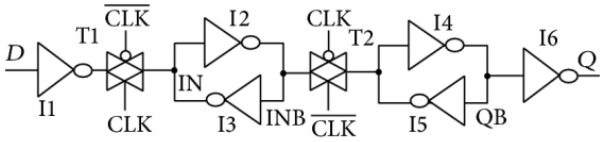


Fig. 15: FinFET flip-flops: transmission-gate [2]

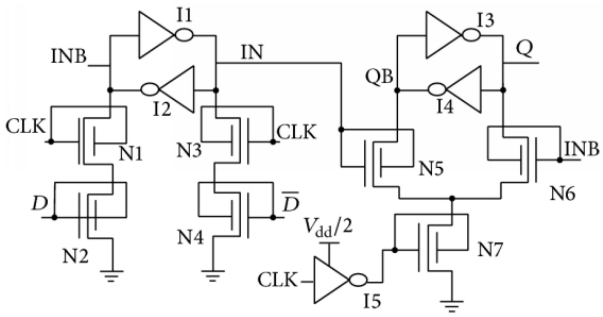


Fig. 16: FinFET flip-flops: half-swing [2]

Numerous studies have looked at different approaches and strategies to develop low-power, high-efficiency flip-flops using FinFET transistors. Using double-gate (DG) FinFETs is one method; these provide less short-channel effects and enhanced electrostatic control over the channel. DG FinFETs may be utilised to create flip-flops with lower power consumption and better performance. Using FinFETs with asymmetric doping profiles is an additional strategy that can enhance flip-flop performance by lowering power and delay. Investigating transistor size, design optimisation, and the use of DG FinFET methods are all part of designing flip-flops

utilising FinFET transistors. Transistor sizing is the process of choosing the FinFET transistors' proper size to get the required power consumption and performance. Design optimisation is the process of searching the design space for the best transistor size and flip-flop architecture. In order to get better performance and lower power consumption, double-gate FinFETs are being investigated through the use of DG FinFET technology. FinFET transistors have been used in a number of research projects to investigate flip-flop design. In contrast to traditional flip-flops, a novel flip-flop design utilising DG FinFETs was suggested in a research that was published in the Journal of Low Power Electronics and Applications. This design achieved a 50% reduction in power usage. A novel flip-flop design utilising asymmetrically doped FinFETs was presented in another research that was published in the IEEE Transactions on Very Large Scale Integration (VLSI) Systems. This design achieved a 30% decrease in power usage over traditional flip-flops. These investigations show how FinFET technology may enhance flip-flop efficiency and performance. To put it briefly, designing flip-flops using FinFET transistors entails investigating a number of approaches and strategies, including transistor scaling, design optimisation, and the use of DG FinFET methods. Compared to conventional planar MOSFET-based flip-flops, the use of FinFET technology in flip-flop design provides the possibility of low power consumption, high speed, and increased performance. FinFET transistors have been used in the design of flip-flops in a number of research projects, showing how this technology may enhance flip-flop efficiency and performance [1] [4] [3].

VII. Numerical Evaluation

A. Theoretical

Device data:

$$N_A = 3 \times 10^1 8cm^{-3}, T_{Si} = 20nm, T_{ox} = 2nm$$

.

1) I-V characteristics:

$$I_d = 2\mu W \times Q_{inv}(y)\frac{\mathrm{d}V_{ch}}{\mathrm{d}y} \tag{11}$$

and we obtain Q_{inv} from the following equation

$$Q_{inv}(y) = Q_{total}(y) - Q_{bulk}(y) \tag{12}$$

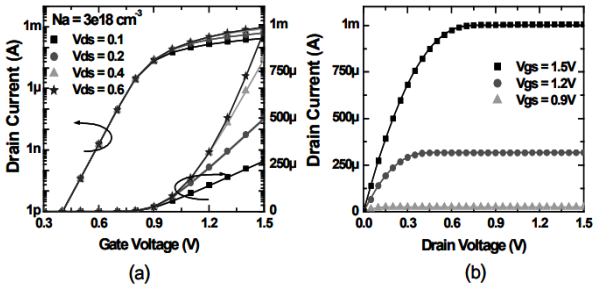


Fig. 17: a. $I_d - V_g$ and b. $I_d - V_d$ characteristics calculated from the I-V model (lines) and TCAD (symbols) [6].

2) Q-V characteristics:

$$B = 2(V_g - V_{fb} - \frac{Q_{bulk}}{C_{ox}} + \frac{2KT}{q}) \tag{13}$$

$$I_d = 2\mu \times \frac{W}{y}(g(\psi_s) - g(\psi_s)(y)) \tag{14}$$

and we obtain $g(\psi_s)$ from the following equation

$$g(\psi_s) = \frac{Q_{inv}^2}{2C_{ox}} + 2\frac{kT}{q}Q_{inv} \tag{15}$$

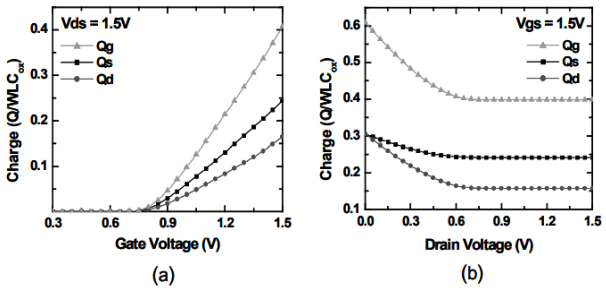


Fig. 18: Terminal charges using Eq. 13 as a function of a. V_{gs} and b. V_{ds} [6].

3) C-V characteristics:

$$C_{ij} = \frac{\partial Q_i}{\partial V_i} \tag{16}$$

and we obtain Q from the following equations:

$$Q_g = 2WLC_{ox}\left(V_{gs} - V_{fb} - \frac{\psi_S + \psi_D}{2} + \frac{(\psi_D - \psi_S)^2}{6(B - \psi_D - \psi_S)}\right) \tag{17}$$

$$Q_d = -2WLC_{ox}\left(\frac{V_{gs} - V_{fb} - \frac{Q_{bulk}}{C_{ox}}}{2} - \frac{\psi_S + \psi_D}{4} + \frac{(\psi_D - \psi_S)^2}{60(B - \psi_D - \psi_S)} + \frac{(5B - 4\psi_D - 6\psi_S)(B - 2\psi_D)(\psi_S - \psi_D)}{60(B - \psi_D - \psi_S)^2}\right) \tag{18}$$

$$Q_s = -(Q_{fg} + Q_{bg} + Q_{bulk} + Q_d) \tag{19}$$

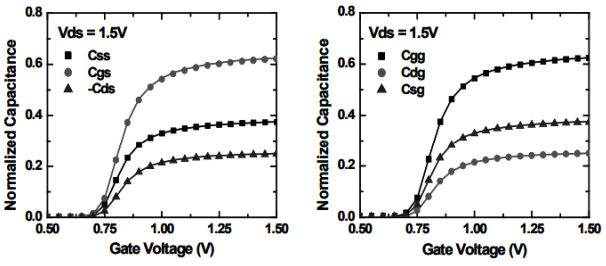


Fig. 19: Capacitances (normalized to $2WLC_{ox}$) calculated from the $C - V$ model (lines) and TCAD (symbols) as a function of V_{gs} [6].

B. Using Computer Simulations: Cadence Virtuoso

In this segment, numerical assessments of the IV equation are incorporated, adhering to the NMOS BSIM-CMG Model and employing Cadence Virtuoso for the analysis.

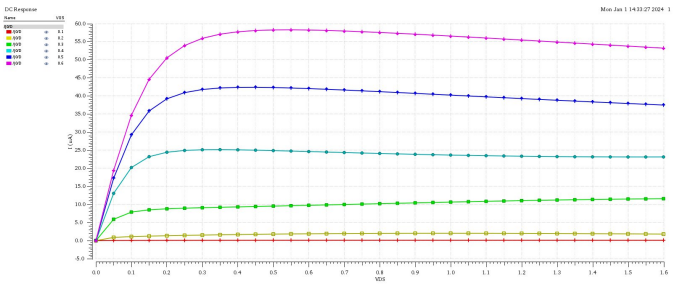


Fig. 20: FinFET characteristics: I_{Drain} and V_{Drain}

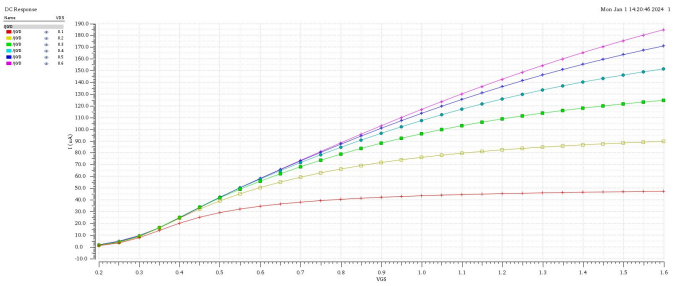


Fig. 21: FinFET characteristics: I_{Drain} and V_{Gate}

VIII. Conclusion

In conclusion, this paper has provided a thorough exploration of FinFET technology, covering key aspects related to drain current modeling, scaling considerations, fabrication challenges, and suitable applications such as SRAM and high-performance computing. The study delved into the intricate details of Drain Current Modeling in FinFETs, shedding light on the complexities involved in characterizing the current flow through the three-dimensional fin structure. This understanding is fundamental for optimizing FinFET performance and ensuring accurate predictions of device behavior. Scaling considerations were extensively addressed, with a focus on mitigating Short Channel Effects (SCE) and optimizing the Contact Gate Pitch. The paper emphasized the crucial scaling relation between fin thickness and channel length to achieve SCE immunity, ensuring the continued success of FinFETs in advancing semiconductor miniaturization. Fabrication problems were identified and discussed, recognizing the challenges in manufacturing FinFET devices. Addressing fabrication issues is pivotal for achieving consistent and reliable production processes, ultimately impacting the scalability and commercial viability of FinFET technology. In summary, this comprehensive examination of FinFETs has provided valuable insights into their modeling, scaling considerations, fabrication challenges, and application suitability. As the semiconductor industry continues to push the boundaries of technology, FinFETs stand out as a promising solution that took the lead as an industry-standard as well as pave the way for future advancements in integrated circuit design. The understanding gained from this paper contributes to the ongoing dialogue on FinFET technology, facilitating its continued evolution and widespread adoption in diverse applications.

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References

[1] S. Kulkarni and S. Patil, "Design of Flip-Flops using FinFET Technology," *International Journal of Engineering Research and Applications*, vol. 7, no. 5, pp. 1-5, 2017.

[2] D. Bhattacharya and N. K. Jha, "FinFETs: From Devices to Architectures," *Advances in Electronics*, vol. 2014, Article ID 365689, pp. 1-21, 2014. https://doi.org/10.1155/2014/365689

[3] Y. Zhang and X. Zhang, "A Low-Power Flip-Flop Design Based on Asymmetrically Doped FinFETs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 2, pp. 743-747, 2016.

[4] Y. Zhang and X. Zhang, "A Low-Power Flip-Flop Design Based on Double-Gate FinFETs," *Journal of Low Power Electronics and Applications*, vol. 5, no. 1, pp. 1-9, 2015.

[5] J. P. Colinge and C. W. Lee, "FinFETs and Other Multi-Gate Transistors," Springer Science & Business Media, 2010.

[6] J. P. Colinge and C. W. Lee, "FinFETs and Other Multi-Gate Transistors," Springer Science & Business Media, 2008.

[7] S. K. Saha, "FinFET Devices for VLSI Circuits and Systems," Routledge, 2020.

[8] M. Alioto, "Comparative evaluation of layout density in 3T, 4T, and MT FinFET standard cells," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 5, pp. 751–762, 2011.

[9] N. Collaert et al., "Tall triple-gate devices with TiN/HfO2 gate stack," *Proceedings of the Symposium on VLSI Technology*, pp. 108–109, June 2005.

[10] A. Agarwal and J. H. Lang, "Foundations of Analog and Digital Electronic Circuits," Morgan Kaufmann, 2005.

[11] B. Holdsworth and C. Woods, "Digital Logic Design," Elsevier India Pvt. Ltd., 2005.

[12] W. J. Dally and R. C. Harting, "Digital Design: A Systems Approach," Cambridge University Press, 2012.

[13] Y. Hayashi, "MOS field effect transistor," JP Patent Application S55-85706, June 24, 1980.

[14] X. Huang et al., "Sub 50-nm FinFET: PMOS," In: *IEEE International Electron Devices Meeting Technical Digest*, pp. 67–70, 1999.

[15] G. E. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, pp. 82-84, April 19, 1965.

[16] Y. S. Chauhan et al., "FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG Standard," Academic Press, San Diego, CA, 2015.

[17] R. H. Dennard et al., "Design of ion-implanted MOSFETs with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. SC-9(5), pp. 256–268, 1974.

[18] S. Cristoloveanu and F. Balestra, "Introduction to SOI technology and transistors," In: *Physics and Operation of Silicon Devices and Integrated Circuits*, J. Gautier, (ed.), ISTE-Wiley, London, UK, New York, 2009.

[19] Y.-K. Choi et al., "Ultrathin-body SOI MOSFET for deep-subtenth micron era," *IEEE Electron Device Letters*, vol. 21(5), pp. 254–255, 2000.

[20] Q. Liu et al., "Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22nm node and beyond," In: *Symposium on VLSI Technology*, pp. 61–62, 2010.

[21] S. K. Saha, "FinFET Devices for Circuits and Systems," CRC Press, 2021.

Appendix A
Simulation Files of FinFET

Find the Cadence Virtuoso PDK model in URL: https://github.com/islamibr/finfet_review_article