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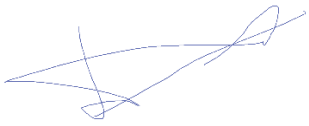
CIRCUIT SOLUTIONS FOR SENSITIVITY INCREASING OF PIEZORESISTIVE PRESSURE SENSORS

Ph.D. thesis abstract

Author: 

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GENERAL DESCRIPTION OF THE THESIS

Relevance of the research. The development of microelectromechanical systems (MEMS) is one of the progressive directions in microelectronics, which will determine the development trends of modern elements and devices. A pressure sensor (PS) is a device, which can convert pressure in an electrical signal. More than 70% of all measurements, which performed by electronic control and information processing systems (in nuclear production, oil and gas industry, car and machine tool building, rocket technology, aviation, transport, medicine, biophysics, thermo- and aerodynamics, acoustics, hydromechanics, geophysics, agriculture and other scientific areas and industry), are associated with measurements of pressure, flow, quantity and level of various liquid and gaseous substances. The main element of PS is a PS chip. The physical parameters of the PS chip are changed depending on the pressure value and type. The accuracy, operational and metrological reliability of an automated process control and management system is largely determined by the quality of sensors, among which the most common are PS with an electrical (analogue or digital) output signal. Strict requirements are imposed on such sensors: high accuracy, miniaturization, sensitivity, mechanical strength, the ability to interface with microelectronic signal converters, long-term stability, low error in temperature characteristics and nonlinearity, as well as a different array of output parameters. The requirements for the PS parameters are fundamentally determined by the possibilities of achieving a precision output signal by PS chip. It obtained by methods known in the literature and, in particular, using the piezoresistive effect on the elements with electrical circuit in the form of Wheatstone bridge (WB). There is a little publication data about the creation of a PS chip with a different electrical circuit, where both piezoresistors (PR) and bipolar junction transistors (BjT) can be used in the composition, which, in turn, can be either deformable BjT (dBjT), and non-deformable BjT. The use of BjT in the electrical circuit of a PS chip can lead to a significant transformation of chip, opening up new possibilities of application in various fields of industry and sciences. Thus, a certain ratio between high sensitivity, reduced chip dimensions and ratio of PS errors allows developing and adapting elements for original equipment manufacturers in the fields of medicine (CPV and spirometry), industrial ventilation systems (variable air flow systems, heating and air conditioning), consumer (drones and smart devices), automotive (exhaust gas circulation and airbag deployment) and other industries (energy and aerospace). Today one of the actual directions in the development of PS is the chip creation for low ranges (below 10 kPa). The applicability of the proposed development is extensive, each of which has certain requirements for sensitive elements in the form of MEMS. Practical significance of thesis in FSUE VNIIA is developing of ultra-highly sensitive small-sized PS

chips for 10 kPa range of differential pressure. All samples of the thesis topic were produced on the technological line of FSUE VNIIA and are available for a visual demonstration of the development.

The goal of this project is the development of technical principles for the creation of piezoresistive PS based on a circuit solution to increase sensitivity and minimize overall dimensions while maintaining input conditions (the geometry of the chip mechanical structure or membrane, supply voltage and low errors of measurement).

It is necessary to consistently solve the following tasks:

1. Substantiate, experimentally confirm and disseminate the application of the piezojunction effect for the creation of piezoresistive PS.

2. Developing of a theoretical model for the operation of PS with an electrical circuit in the form of a piezoresistive differential amplifier (PDA) and piezoresistive differential amplifier with negative feedback loop (PDA-NFL), taking into account the reasonable use of piezoresistive and piezojunction effects. Substantiate proposals for increasing sensitivity and reducing errors in terms of temperature and noise dependence of the output signal.

3. Developing of a series of PS chip topologies and technological routes for a number of modifications of PS chips with proposed circuit solutions.

4. Research the output characteristics of PDA and PDA-NFL PS chip in a comparative analysis relative to analogues with a WB circuit for 60, 160 and 600 kPa pressure ranges of differential pressure.

5. Modernize the design of the ultra-highly sensitive small-sized PDA-NFL PS chip with the most efficient design and circuitry solution for 10 kPa range of differential pressure.

Scientific provisions and results submitted for protection:

1. A circuit solution of piezoresistive PS chip by PDA-NFL circuit, which is distinguished by the use of amplifiers in the two circuit branches and the use of eight PRs in the base, emitter, collector parts of amplifier, which provides a sensitivity increase by 3.5 times relative to the use of WB circuit.

2. A design and technological solution for PS chip with PDA-NFL circuit, characterized in that a topological structure is technologically implemented, in accordance with patent No. RU 195159, where areas of compression and tension mechanical stresses contain eight PRs of p-type conductivity and two non-deformable BjTs with a vertical structure of npn-type conductivity, which ensures a reduction in overall dimensions of at least 2.4 times while maintaining sensitivity relative to a PS chip with WB circuit.

Scientific novelty of the thesis:

1. The piezojunction effect of a deformable BjT as part of electrical circuits of silicon PS chip has been experimentally confirmed and disseminated.

2. The theoretical design PS chip has been proposed due to the use of original PDA-NFL circuit solutions, which allows sensitivity increase by 3.9 times relative WB circuit and by 2.9 times relative to PDA circuit.

3. The experimental design and technological solutions were proposed for creating PS chip with PDA-NFL circuit, among which the most effective solution is the use of a non-deformable BjT with a vertical structure of npn-type conductivity, which makes it possible to increase the sensitivity relative to analogues with WB circuit by 3.5 times or reduce area of PS chip by 2.4 times, as well as increase the sensitivity relative to analogs with PDA circuit by 2.8 times, reduce errors of temperature characteristic by more than an order and reduce the noise of the output signal by 20 times.

The practical significance of the thesis:

1. PS chips with PDA circuit and dBjT have been created. The sensitivity of PS chips with PDA circuit is 2.2 times higher relative to the analogue (TMU18) with WB circuit.

2. PS chips with PDA-NFL circuit and BjT with a vertical structure of the npn-type (V-NPN) or BjT with a lateral structure of the pnp-type (L-PNP) have been created. The sensitivity of PS chips are 3.5 times or 2.2 times higher, respectively, relative to the analogue (IPD60) with WB circuit. An analysis of the output characteristics of PDA-NFL chip (V-NPN) proved the possibility of reducing the overall dimensions by 2.4 times relative to its analogue (IPD52) with WB circuit, while maintaining the sensitivity.

3. PS chips with PDA-NFL circuit (V-NPN) for the practical significance of thesis in FSUE VNIIA has been created. The development for measurement of differential range to 10 kPa is applicable to the nuclear and oil-gas industries. The study of batch confirmed the possibility of simultaneously increasing the sensitivity by 5.8 times and reducing the chip area by 2.4 times relative to the analogue (IPD52) with WB circuit. The supply voltage, the measured pressure ranges up to 10 kPa and low errors are maintained.

As a result of the research, 5 samples of PS chips with PDA-NFL circuit (V-NPN) in cases were transferred for use as sensitive elements in full construction of pressure sensors. Patents No. RU 195159 U1 dated June 13, 2019 and No. RU 195160 U1 dated June 13, 2019 were obtained for results protection. The use of patents is documented by the “Act on the implementation of the result of intellectual activity No. T0522-05/028-2022 dated June 24, 2022 and No. T0522-05/029-2022 dated June 24, 2022 at FSUE VNIIA.

Personal contribution of the author. The author made the choice of research objects, set goals and objectives, chose methods; obtained, processed and analyzed the results of experiments. The study was conducted personally by the author. All experimental results, their processing and analysis presented in the thesis and were obtained by the author personally.

Approbation of the thesis results. The main thesis results were reported at IEEE Sensors (Sydney, Australia, 2021), XII International Scientific and Technical Conference "Micro- and Nanotechnologies in Electronics" (Elbrus, Russia, 2021), XIV and XIII Russian Conference on Physics Semiconductors (Novosibirsk, Russia, 2019 and Yekaterinburg, Russia, 2017), XIII, XII, XI and VIII Scientific and Technical Conference "VNIIA" (Moscow, Russia, 2019, 2018, 2017 and 2014), V All-Russian scientific conference with international participation "Actual problems of micro- and nanoelectronics" (Ufa, Russia, 2018).

Published thesis results. 6 articles were published in international journals indexed by the Scopus and Web of Science systems (Sensors and Actuators A: Physical, IEEE Sensors Journal, IOP Journal of Micromechanics and Microengineering, IOP Physics Script), 2 articles in Russian journals recommended by the Higher Attestation Commission (Nano- and Microsystem Technology, Sensors and Systems), 5 Russian patents, 1 article of international conferences indexed by Scopus and Web of Science systems, 8 abstracts in collections of Russian scientific conferences.

The structure and scope of the thesis. The thesis consists of an Introduction, 4 Chapters, Conclusions, References with 230 titles, 1 Appendix. The thesis is presented on 178 pages with 88 Figures, 33 Tables and 52 Equations.

THE CONTENT OF WORK

Introduction contains relevance justification of the research topic, provides a brief description of problems, describes the goal, scientific novelty, shows the thesis structure, outlines the main scientific provisions submitted for protection.

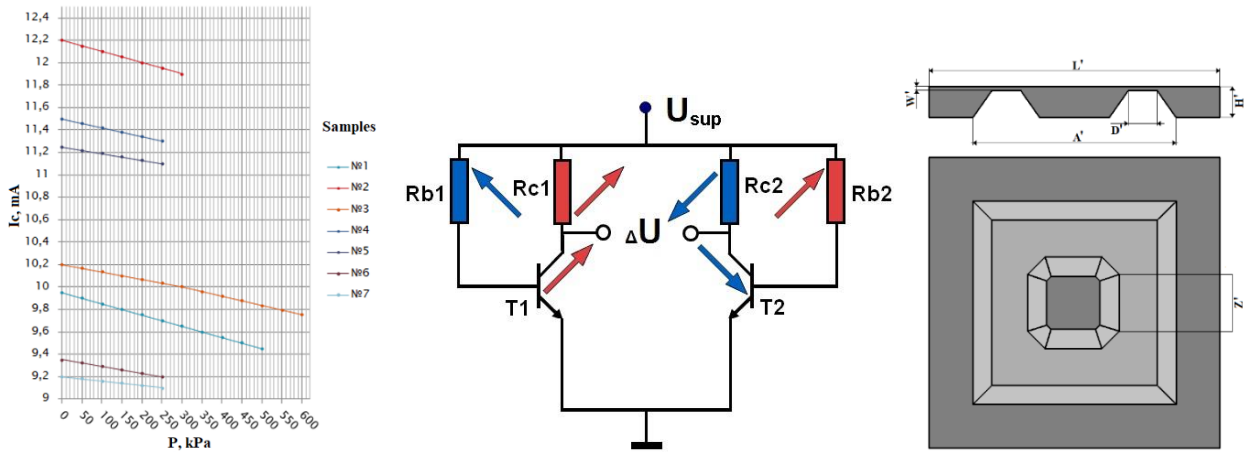
Chapter I is devoted to an overview of advantages and disadvantages of PS chip creation operating on piezoresistive effect and using WB circuit with 4 PRs in order to achieve output parameters that include the required sensitivity for low ranges of pressure up to 10 kPa (and below) [1-3]. These researches have the lowest possible measurement errors in terms of non-linearity, temperature coefficient, as well as mechanical hysteresis and repeatability. The output characteristics of such developments [4-7] directly depend on the overall dimensions of PS chips, and, as a consequence, the membrane, as well as the geometric structure of the membrane, where the mechanical stress (MS) compensators can have any shape with different location of

PRs on a thinned part of membrane. The limit of possibilities for PS chips with similar membrane structures can be significantly improved by changing the topological pattern with a different electrical circuit. In addition, analogs of PS chips and sensitive elements of MS were analyzed using various deformable structures of active elements - these are dBjT [8-10] and deformable metal-oxide-semiconductor transistor (dMOSFET) [11, 12]. The chapter shows the principles of functioning for deformable transistors, both in a single version and as part of various electrical circuits. The main advantage of developments using WB circuit with dMOSFETs, a current mirror circuit with an dBjTs and a single dMOSFET is the possibility of a multiple reduction of chip areas and the precise arrangement of transistors in the regions of maximum MS. The design principles, technological features and optimization of the output characteristics (sensitivity, temperature dependence, and others) are also discussed. The greatest interest in the use of dBjT for PS chips was presented in early works (1980s) by a research group from MEPhI led by Vaganov V.I. [8,9], where a PDA circuit with dBjTs and PRs is used. The authors draw the following conclusion about the advantages of the development: “thus, the problem of sensitivity increasing of PS chip while maintaining the size, or reducing the size chip while maintaining the sensitivity is solved. In addition, it is possible: a) to increase the power of the output signal due to the greater distribution of components over the surface; b) improve the temperature stability, c) improve the threshold sensitivity.” Despite this weakly substantiated statement, the idea of development was at the initial stage, because there are no: 1) a comparative analysis with a PS chip utilizing WB circuit and same membrane structure; 2) a theoretical model of the strain effect in dBjT (or piezojunction effect) and PR, as well as the operation of the full-fledged electrical circuit; 3) consideration of more advanced technological possibilities for the implementation of PS chips at the moment; 4) consideration of more relevant topological constructions for the top side and structural construction for the back side of PS chip; 5) a detailed study of an extensive list of input and output characteristics of PS chip in a statistical analysis of an array of samples; 6) proposals and justifications for reducing the errors of PS chips, which are not mentioned in these works. Unfortunately, after more than 40 years, this idea was not developed. Research of thesis, based on the use of a new electrical circuit with BjT. Research will demonstrate in detail and prove the achievement of significant advantages of the development (high sensitivity, small dimensions, low errors and high protection by overload pressure) and minimizing the main error factors (temperature characteristics and noise component of the output signal).

Chapter II demonstrates the fundamental mechanism of the influence on electrical parameters in silicon structures by mechanical deformation. The main determining parameter of the piezoeffect in the structures of PR and dBjT is the mobility of charge carriers within the

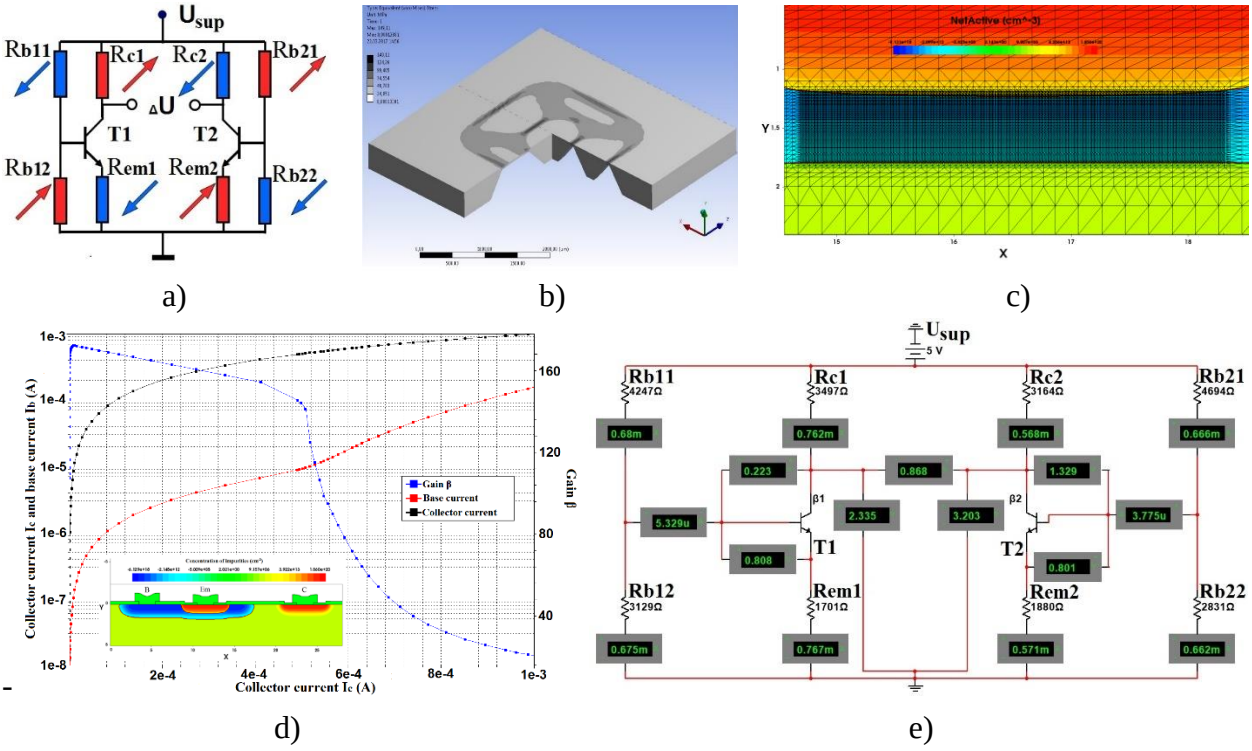
limits of MS up to 1 GPa. The change of mobility for the majority and minor charge carriers depends on the MS values, as well as the choice of the crystallographic plane (CGP) for wafer, crystallographic direction (CGD), and the type of conductivity. The piezoresistive effect on PR (used in a variety of PS chips for mass production and research) is based on the mobility changing of the majority charge carriers and is presented in this chapter. There is another little-known theory of the piezojunction effect for dBjT, where changes in current-voltage (I-V) characteristics under the influence of MS occur due to a change in the mobility of minority charge carriers in the base region. The term "piezojunction effect" was first used by a group of researchers F. Fruett and G. Meijer from TU Delft at the beginning of 2000 [11]. The chapter demonstrates in detail the physical substantiation of the piezojunction effect for two types of dBjT structures: vertical structure of npn-type conductivity (V-NPN) and lateral structure of pnp-type conductivity (L-PNP). As in the case of the piezoresistive effect, the concepts of the piezojunction coefficient (for the collector current) were introduced, which also depends on the choice of CGP, CGD and the type of dBjT structure. The practical part of the thesis begins with experimental confirmation of piezojunction effect (Fig. 1a), using the sample of dBjT V-NPN. The calculation of the piezojunction coefficient has been made. The piezojunction coefficient significantly depends on the technological and topological features of the dBjT structure: the experiment proves the achievement of $\xi^{V\text{-}NPN}_{ijkm} = 0.89 \cdot 10^{-10}$ Pa^{-1}, the values of the research team from TU Delft $\xi^{V\text{-}NPN}_{ijkm} = 0.80 \cdot 10^{-10}$ Pa^{-1}). After that a theoretical model for the piezoresistive effect and analyzing MS values in the membrane structure (by ANSYS) was demonstrated in a comparative analysis with experimental data. The theories of piezojunction and piezoresistive effects were used to construct a theoretical model for PS chip with a new PDA electrical circuit (Fig. 1b), which has its own input parametric values for dBjT V-NPN and PR, and with a more relevant membrane structure (with one right island (RI), Fig. 1c). PS chip with PDA circuit looks like the prototype [8,9] from Chapter I. Additionally, two main potential disadvantages are indicated in terms of temperature characteristics and the noise component of the output signal. The possibility of sensitivity increasing by 2.2 times relative to PS chip with WB circuit has been proven. This advantage is achieved while maintaining the input parameters, such as the pressure range, supply voltage, the design of the mechanical part and overall dimensions. Additionally, the influence of temperature change can critically influence on the output signal with the temperature coefficient of the zero signal TCZ = 3.4 %/10 ºC.

A radically new circuit design solution was proposed for the implementation of PS chip with transistors. The PDA electrical circuit has been improved by using negative feedback loop (NFL) (Fig. 2a).



a) b) c)

Figure 1. PS chip with PDA circuit: a) changes in the dBjT V-NPN collector current on pressure $\Delta I_C(\Delta P)$, b) PDA electrical circuit, c) geometry of the back side (membrane)



a) b) c)

d) e)

Figure 2. PS chip with PDA-NFL circuit (example with BjT V-NPN for 60 kPa range; similar models were also completely created for BjT L-PNP and other pressure ranges): a) PDA-NFL electrical circuit with dBjT V-NPN, b) MS distribution (Mises) in the membrane structure by ANSYS, c) the thickness of the active base region by Synopsys TCAD , d) BjT structure and I–V characteristics of $I_C(U_B–U_E)$, $I_B(U_B–U_E)$ and gain $\beta(U_B–U_E)$ by Synopsys TCAD, e) distribution values of resistance, currents and voltage drops under pressure ΔP = 100 kPa (pressure is applied from the back side of PS chip)

Such a circuit solution allows more efficient redistribution of currents and potentials in the electrical circuit to increase sensitivity (while maintaining the geometry of the membrane, supply

voltage U_{sup} = 5V and by increasing the number of PR from 4 to 8) and thermal compensation of the output signal (due to stabilization of the temperature dependence for base-emitter voltage drop on dBjT). Any circuit solution should also logically evaluate the possibilities of practical implementation of such electrical connections for semiconductor structures with the currently available technological capabilities of fabrication line. A more detailed theoretical model for 4 types of PDA-NFL circuits was built using dBjT and non-deformable BjT with V-NPN and L-PNP structures, based on: 1) analytical calculation of the resistance values for PRs (four type TR $R_{B11(21)}$, $R_{B12(22)}$, $R_{Em1(Em2)}$ and $R_{C1(C2)}$ in pairs have their own values in contrast to WB circuit with same values for all PRs) and BjT operating points. There is a certain set of PR resistance values for BjT V-NPN or BjT L-PNP. It is necessary for a balanced ratio between high sensitivity, low temperature error and low noise component of the output signal; 2) detailed mode of diffusion processes for the technological route and analysis of I–V characteristics of BjT in Synopsys TCAD, taking into account the creation of two types of BjT and PR on a single silicon wafer (Fig. 2b). The noise decreasing of the output signal for PS chip with PDA-NFL circuit occurs due to thickness decreasing of the BjT active base region, where recombination of minority carriers is observed (causing Flicker noise, Fig. 2c); 3) analysis of maximum MS areas in a membrane structure with three RIs for three types of pressure ranges by ANSYS (Fig. 2d); 4) determination of output characteristics by sensitivity and additional temperature error due simulating PDA-NFL circuit behavior by NI Multisim (Figure 2e).

Researches were carried out to theoretically confirm the advantages of the proposed circuit solutions for PS chip with PDA-NFL circuit. A comparative analysis with WB and PDA circuits proved the relevance of using a radically new PDA-NFL electrical circuit:

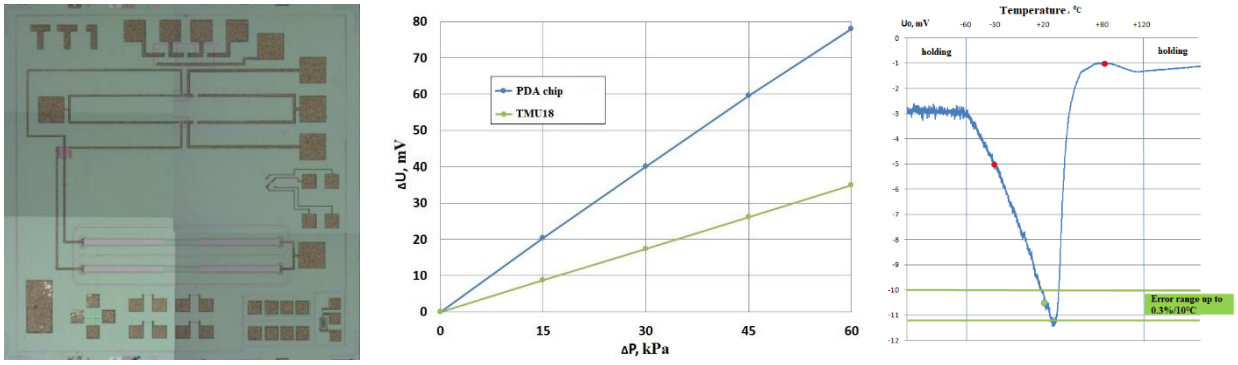
a. The PS chips with PDA-NFL circuit utilizing BjT V-NPN and BjT L-PNP have significant advantages of relative prototype with PDA circuit. This is sensitivity increasing by 2.9 times and 2.3 times, as well as a reduction in the additional component TCZ by 15 times and 6 times, respectively. This is achieved by maintaining the supply voltage, overall dimensions and pressure range (60 kPa);

b. The PS chips with PDA-NFL circuit utilizing BjT V-NPN and BjT L-PNP have significant advantages of relative prototype with WB circuit for three types of differential pressure ranges up to 60, 160 and 600 kPa. The sensitivity increases by 3.9 times and 3.3 times, respectively, on average for all ranges.

The PS chip with PDA-NFL circuit utilizing BjT V-NPN has significant advantages of a relative sensitive elements of MS with current mirror electrical circuit with four dBjT L-PNP [10]. Sensitivity of the development increases by 2.4 times while maintaining MS values. The

same situations relative to PS chip with dMOSFETs as part of half sensitive WB electrical circuit [11]. Sensitivity of the development increases by 11 times while maintaining MS values.

Chapter III. The structure of PDA chip was chosen after discussing a variation of 4 topologies and describing the technological route (Fig. 3a). A comparative analysis of the output characteristics for PDA chip was carried out relative to an analogue with WB circuit (TMU18). This analogue has identical geometry of the mechanical part. The performance of 11 PDA chip samples for 60 kPa pressure range demonstrated the achievement of sensitivity S_{PDA} = 0.66 ± 0.05 mV/kPa/V, which is on average 2.2 times higher than sensitivity of analogue (Fig. 3b).



a) b) c)

Figure 3. PDA chip: a) top side, b) dependency of output signal on pressure (in comparison with TMU18), c) example dependency of output signal on temperature

Two main disadvantages of development were identified. This is a high error in temperature characteristics (TCZ = 2.5 ± 1.3 %/10 °C, TCS = 2.9 ± 0.3 %/10 °C, THZ = 6.2 ± 3.6 % and THS = 2.0 ± 0.9 %, which is significantly higher than errors of TMU18 chip, Fig. 3c) and the noise of output signal (U_{noise} = ±300 μV, which is more than 100 times higher than the value of TMU18 chip). It is also necessary to note the increase in the imbalance of output signal due to more elements in the circuit and, in particular, due to the dBjT ($|U_0|$ < 100 mV).

9 types of topology for PDA-NFL chips were developed based on the theoretical model and an improved technological route (Fig. 4). The topologies of PDA-NFL chip differ in: 1) the choice of BjT structure V-NPN or L-PNP and, accordingly, the values of TR; 2) tangential and radial location of the dBjT base area; 3) using a reduced nominal resistance to the emitter region R_{Em} for BjT L-PNP. It is necessary for decreasing of parasitic current component into the substrate from the emitter-epitax-substrate transistor; 4) the location of BjT on the deformable and non-deformable area of membrane. 3 types structure mechanical structure (for pressure ranges up to 60, 160 and 600 kPa) for PDA-NFL chip were used for all 9 types of topologies.

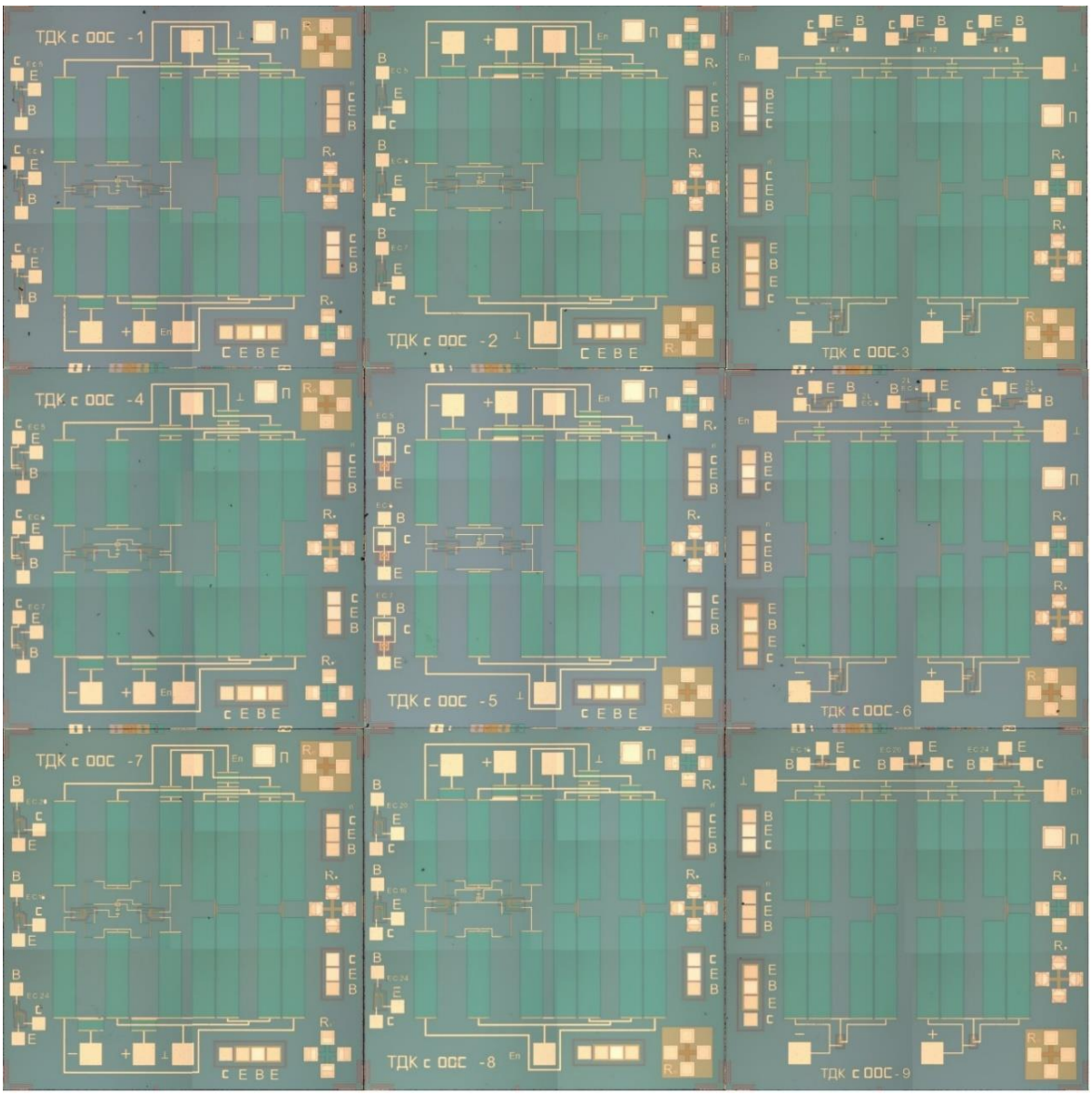


Figure 4. 9 types of topologies for PDA-NFL circuit

The dBjT had to be compactly located in the region of maximum MS ($A_{MN} \approx 40 \times 400$ μm^2) together with PRs in topologies No. 1, 2, 4, 5, 7 and 8. The placement of dBjT had to be in the limited area within guard ring (silicon wafers with an epitaxial structure were used). The dBjT contacts are formed without metallization on the thinned part of membrane. Contacts between dBjT and metallization is made by highly doped conductor regions (Fig. 5). The designed gap (d = 10 μm) between the highly doped conductor regions was used with mistake. It is necessary to take into account many factors related to: 1) the width of silicon oxide etching wedge by photolithography, 2) lateral impurity diffusion, 3) the space charge regions (SCR) at given circuit potentials. The crossing of SCR between neighboring highly alloyed conductor regions of dBjT breaks down the operation of PDA-NFL circuit. It led to the failure of topologies No. 1, 2, 4, 5, 7 and 8. The calculation in detail showed that the minimum gap between areas should be more than d > 12 μm.

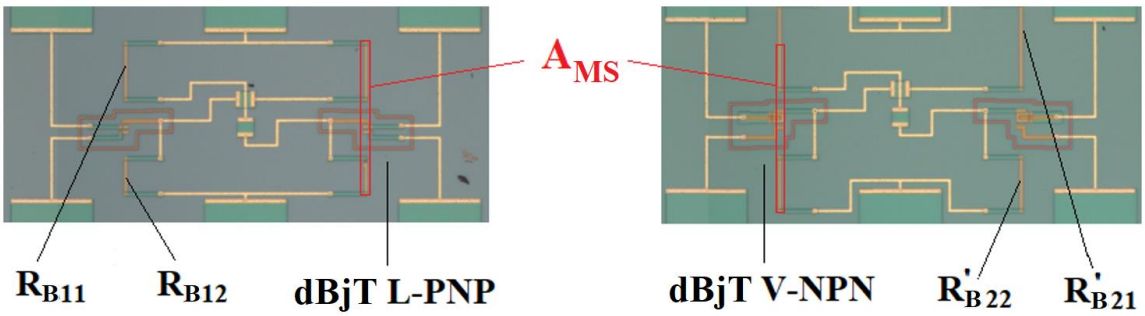


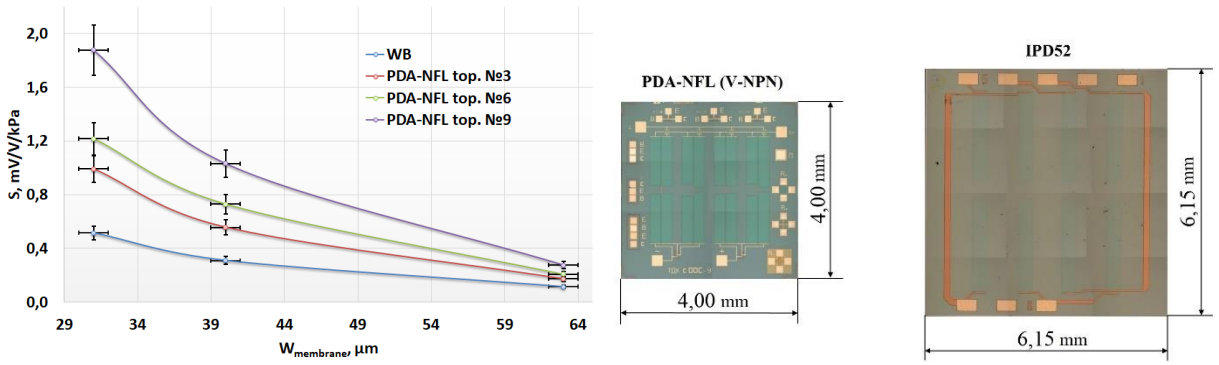
Figure 5. Location of dBjTs and PRs on the thinned part of membrane

Topology No. 3 with non-deformable BjT L-PNP and R_{em} = 4.5 kOhm, topology No. 6 with non-deformable BjT L-PNP and R_{Em} = 1.5 kOhm and topology No. 9 with non-deformable BjT V-NPN were successfully completed. The difference between the using of dBjT and non-deformable BjT in these electrical circuits is from 1 to 5% (better for dBjT), as has been shown by pressure output analysis in NI Multisim. But, as practice has shown, the development of topologies itself (which taking into account all the features for arrangement of elements in a limited area of maximum MS) leads to a significant complicating the arrangement of circuit elements.

All the output characteristics of PDA-NFL chip will be presented in a comparative analysis with WB chip (IPD60) and with same area and geometric parameters of membrane structure. IPD60 is the commercially produced PS chip at VNIIA. PDA-NFL chip were assembled into a silicon structure to remove residual MS and hermetically apply pressure from one of the chip sides. Then this silicon construction connects with a case of PS module for subsequent measurement. In Tab. 1 and in Fig. 6a shows the dependences of sensitivity on membrane thickness (the main influencing parameter on the sensitivity to achieve certain ranges) for three types of PDA-NFL chips and WB chips. The length of RI edge for PDA-NFL chips is about Z = 490 ± 50 μm; the gap between two RIs or RI and non-deformable chip frame is about D = 58 ± 3 μm. It can be seen that the PDA-NFL chips with topologies No. 3, 6 and 9 have, on average, 1.7, 2.2 and 3.5 times, respectively, higher pressure sensitivity than WB chip (IPD60).

Table 1. Sensitivity for three types of PDA-NFL chips relative to IPD60 and PDA chip

Type of chip	Membrane thickness $W_{membrane}$, μm	Sensitivity S, mV/V/kPa			
		PDA-NFL, topology No. 3	PDA-NFL, topology No. 6	PDA-NFL, topology No. 9	PDA
60 kPa	31.0±1.5	0.991 ± 0.098	1.216 ± 0.149	1.877±0.116	0.515 ± 0.049
160 kPa	40.0±1.5	0.556 ± 0.041	0.729 ± 0.045	1.031 ± 0.097	0.310 ± 0.033
600 kPa	63.0±1.5	0.172 ± 0.017	0.208±0.025	0.398 ± 0.044	0.115 ± 0.009



a) b)

Figure 6. PDA-NFL chip: a) dependences of sensitivity on membrane thickness (or range) for three types of PDA-NFL chip relative to WB chip (IPD60), b) an example of reducing the PDA-NFL chip area by 2.4 times relative to WB chip (IPD52) while maintaining the sensitivity and nominal thickness of membrane thinned part

The possibility of reducing the chip area by 2.4 times and increasing of burst pressure by 5.2 times ($P_{Burst\ PDA\text{-}NFL}$ = 1.6 MPa) relative to the PS chip (IPD52) with WB circuit is demonstrated (Fig. 6b). It happened while maintaining sensitivity S = 1.9 mV/V/kPa and the thickness of membrane thinned part (W = 35 µm). The output unbalance limits were taken equal to $|U_{0\ PDA\text{-}NFL}| < 60$ mV due to the balancing needs of 8 PRs and 2 BjTs. The high values of noise for output signal (frequency range is about tens of kilohertz) was reduced from $\Delta U_{PDA\ noise} = \pm 300$ µV to $\Delta U_{PDA\text{-}NFL\ noise\ No.\ 9} = \pm 15$ µV. Noise reduces the previous values of PDA chip by 20 times. It is only 6 times higher than the values of WB chip. The parameters was studied by errors PS chips as part of assembly structures for the most relevant for consideration range (60 kPa) due to sharper dependences of errors and having a larger number of samples for statistics (topology No. 3 - 22 samples, No. 6 - 28 samples and No. 9 - 20 samples). In addition to the sensitivity advantage, the PDA-NFL chip topology No. 9 with BjT V-NPN has a much better ratio between the parameters of elements to achieve low errors in 8 temperature characteristics as compared to PDA-NFL chip topologies No. 3 and No. 6 with BjT L-PNP. The temperature characteristics of PDA-NFL chip topology No. 9 with BjT V-NPN still remain higher than the similar values for WB chip (IPD60), but these values were reduced by more than an order relative to the prototype PDA and analogue PDA-NFL chip topologies No. 3 and No. 6 with BjT L-PNP. If we assess the excess of errors of temperature characteristics only in the “minus” temperature range (from +20 ^{0}C to -30 ^{0}C), we observe an acceptably small increase in THZ by 2.2 times, THS by 1.8 times and TCZ by 2.7 times, as well as a decrease in TCS by 1.3 times. The reason for the higher excesses of temperature characteristics in the “plus” range is the increasing speed for the transition of V-NPN BjT to the saturation mode at T > +60 ^{0}C. Thus, the

most attractive range for temperature characteristics of PDA-NFL chip topology No. 9 with BjT V-NPN is the “plus” region with a lower upper limit from T = +80 ^{0}C to T = +60 ^{0}C, in which THZ decreases by 2.0 times, THS decreases by 1.3 times, TCZ decreases by 2.0 times and TCS decreases by 1.9 times. Thus, in the “plus” temperature range (up to T = +60 ^{0}C) we observe a small increase in THZ by 1.3 times, THS by 1.2 times, TCZ by 2.9 times and TCS by 1.5 times relative to analogue WB chip (IPD60). PDA-NFL chip topology No. 9 with BjT V-NPN with the most efficiently built electric topology has temperature errors no more than an order higher relative to WB chip, as it was previously demonstrated on the prototype PDA chip. All temperature errors have only 1.5-2.5 times higher values and does not exceed the limits of 0.3% for THZ and THS and 0.3 %/10 ^{0}C for the TCZ in the temperature range from -30 to +60 ^{0}C. Additionally, the errors of PDA-NFL chip topology No. 9 with BjT V-NPN were considered in terms of nonlinearity, influence of mechanical strength, the effect of all-round compression by pressure and long-term stability. The nonlinearity of PDA-NFL chip topology No. 9 with BjT V-NPN has a parameter 1.7 times lower than the parameters of WB chip, which indicates a significant advantage of this development. The error of zero signal changing of PDA-NFL chip topology No. 9 with BjT V-NPN under the influence of overload pressure from both chip sides, as well as under the action of all-round compression, remains equal to the parameter for WB chip. The long-term stability of PDA-NFL chip topology No. 9 with BjT V-NPN increased by 3.0 for zero output signal, and 1.8 times for sensitivity relative to WB chip due to the presence of BjT in the circuit. But at the same time errors does not exceed the limit of 0.1%.

Chapter IV considers the actual possibility of using a new PDA-NFL electrical circuit to create an ultra-highly sensitive small-sized PS chip for low pressure ranges. The proposed type of development of an ultra-highly sensitive small-sized PDA-NFL chip is used as part of the assembly structure of pressure sensor for differential pressure up to 10 kPa, which commercially produced at FSUE VNIIA. The parameters of ultra-highly sensitive small-sized PDA-NFL chip for 10 kPa will be analyzed with the characteristics of WB chip (IPD52), which commercially produced at FSUE VNIIA. The chapter substantiates the reasons for the actual limit in design of PDA-NFL chip for 10 kPa, where it is necessary to simultaneously fulfill the requirements for achieving sensitivity and an array of various low errors. The main task in modeling is showing of: how to change the geometry of mechanical part to achieve significantly higher output sensitivity readings (more than 5 times) for 10 kPa range with reduced area of 2.4 times relative to IPD52 chip. The most relevant topological structure №9 of PDA-NFL with non-deformable BjT V-NPN (Fig. 7a) is used according to the results obtained in Chapter III. The design of mechanical part (membrane) is modernized for low pressure range (10 kPa). The theoretical model is corrected for the use of other values of MS with the modified design of membrane for

PDA-NFL chip. The topological pattern of top side is optimized while maintaining the geometric arrangement of PRs and BjTs. Epitaxial structures of silicon wafers and the technological route, which was determined earlier as a result of simulation by Synopsys TCAD according to doped impurity distribution maps for each of the regions separately and for the BjT structures, as well as their I–V characteristics, and confirmed experimentally, completely coincides with PDA-NFL chip for higher ranges. Additionally, a thin supermembrane oxide (SO) W $_{SIO2}$ = 55 nm is created above the thin part of membrane. It is necessary for decreasing of potential effect by residual MS on the main parameters of PDA-NFL chip.

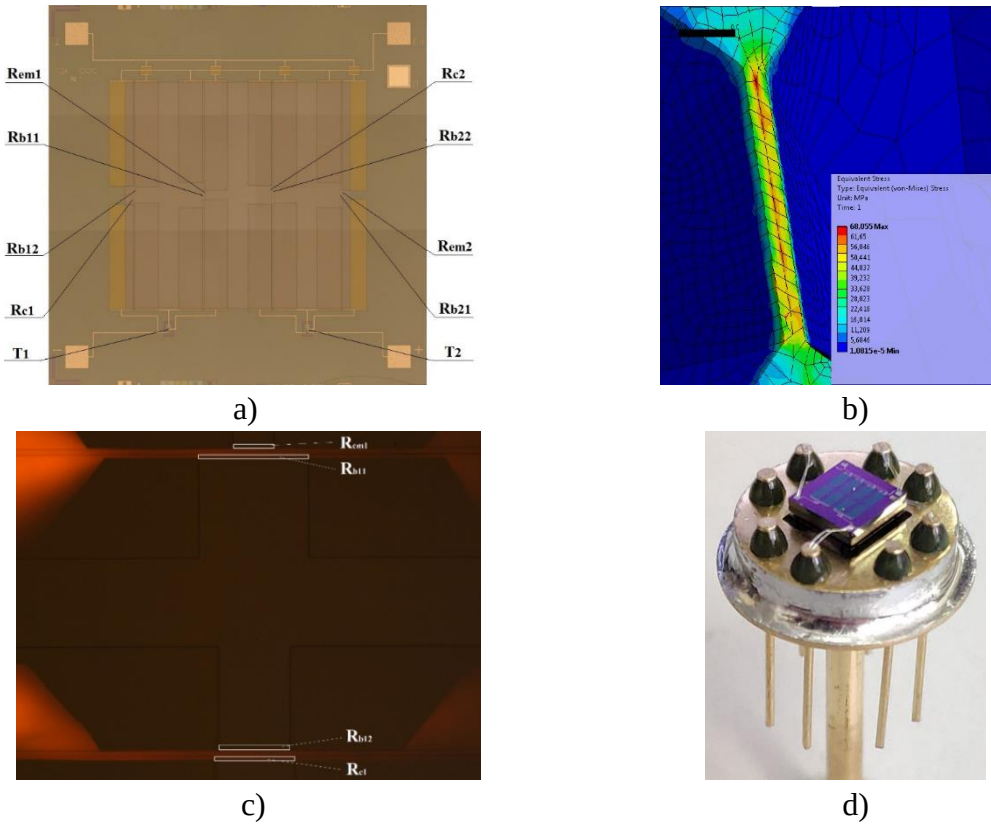


Figure 7. PDA-NFL chip for 10 kPa range: a) top side, b) map of MS distribution between two RIs, c) illuminated sector with the location of PRs relative to RI zones (R_C is the longest PR), d) assembly of PS module

The possibilities of changing the geometry of mechanical part with a similar structure as for 60, 160 and 600 kPa ranges were analyzed (three RIs, liquid anisotropic etching with a small part of isotropic etching at the final stage). There is the variation of three main parameters: edge length RI Z, the gap between the RIs or RI and the chip frame D, as well as the thickness of membrane thinned part W (Fig. 7b). MS equals σ_j = 51.2 MPa (according to von Mises) when applying pressure ΔP = 10 kPa from the back side. It achieves when the thickness of thinned part W = 10 μm, the length of the thinned part for square membrane A = 2260 μm and with distribution areas of maximum MS between stress concentrators (ZxD = 800x26 μm^2). The

relative change in resistance was calculated using the theory of the piezoresistive effect for PR. The relative change in resistance is dR_i = 3.2%, and the theoretical sensitivity indicators for the electrical circuit of PDA-NFL by NI Multisim is calculated. $S_{\text{theor PDA-NFL 10 kPa}}$ = 11.1 mV/V/kPa and additional temperature error $TCZ_{\text{theor PDA-NFL 10 kPa}}$ = 0.04 %/10 ^{0}C. Figure 7c shows a photo of the membrane sector for the ultra-highly sensitive small-sized PDA-NFL chip. The location of PRs is visible on the thinned part between RIs.

The ultra-highly sensitive small-sized PDA-NFL chip for 10 kPa were assembled into a silicon structure as in the case of analogues for large ranges. After that the silicone structure is placed into the case of PS module (Fig. 7d). 18 working samples of PS modules with PDA-NFL chip were obtained. The output characteristics is considered relative to module PS with IPD52 chip (14 samples). All parameters are analyzed under the condition when pressure is supplied from each chip side. Initially, we must note the input advantage in reducing the PDA-NFL chip area by 2.4 times, equal to 4.00x4.00 mm^2, relative to the IPD52 chip area, equal to 6.15x6.15 mm^2. The limits of zero output for PDA-NFL chip for 10 kPa have been claimed up to $|U_{0\ \text{PDA-NFL for 10 kPa}}| < 30$ mV. The sensitivity of PDA-NFL chip for 10 kPa is $S_{\text{PDA-NFL chip for 10 kPa}}$ = 10.19 ± 2.31 mV/V/kPa on average relative to two types of pressure supply (from the side of the membrane and from the top side) or $\Delta U_{\text{PDA-NFL chip for 10 kPa}}$ = 509.7 ± 115.6 mV at U_{sup} = 5 V and pressure ΔP = 10 kPa, which is 5.8 times higher than on the analogue IPD52 chip, where $S_{\text{IPD52 for 10 kPa}}$ = 1.76 ± 0.30 mV/V/kPa or $\Delta U_{\text{IPD52 for 10 kPa}}$ = 87.9 ± 14.9 mV with U_{sup} = 5 V and pressure ΔP = 10 kPa. The nonlinearity of PDA-NFL chip for 10 kPa is $2K_{\text{NL PDA-NFL chip for 10 kPa}}$ = 0.26 ± 0.12% on average with respect to two types of pressure supply (from the side of the membrane and from the top side), which in 6.5 times higher than on the analogue IPD52 chip, where $2K_{\text{NL IPD52 for 10 kPa}}$ = 0.04 ± 0.02%, but PDA-NFL chip for 10 kPa satisfies the conditions stated for development ($2K_{NL}$ < 0.50%). A graph of output signal changing and nonlinearity on applied pressure is shown in Fig. 8.

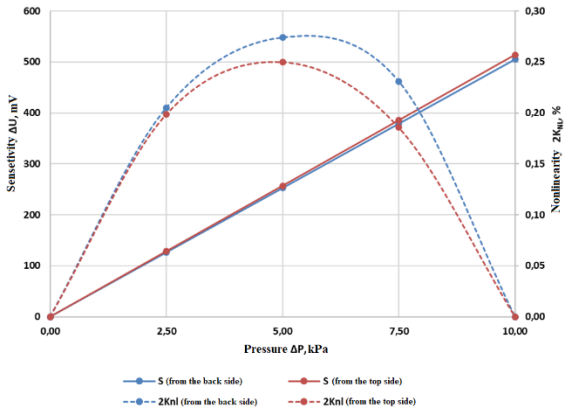
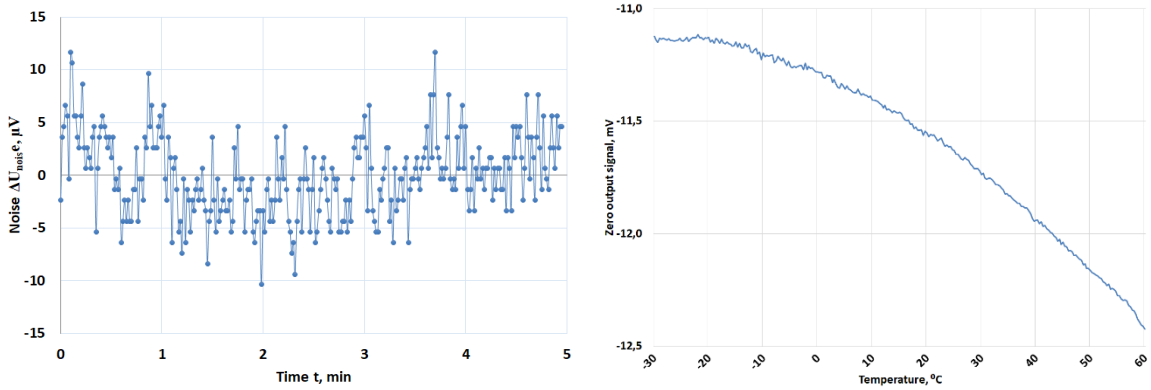


Figure 8. Graph of dependence of output signal changing and nonlinearity on applied pressure for PDA-NFL chip for 10 kPa

The noise of output signal of PDA-NFL chip for 10 kPa is $\Delta U_{\text{noise PDA-NFL chip for 10 kPa}} = \pm$ 15 μV (Fig. 9a) and equals to analogue for higher ranges from Chapter III. There is actually a similar ratio of the useful signal by applied pressure to the noise component of output signal for two types of PS modules with different chips: $\Delta U_{\text{PDA-NFL for 10 kPa}}/\Delta U_{\text{noise PDA-NFL for 10 kPa}} = 509{,}7 \cdot 10^3/15 \approx 3{,}4 \cdot 10^4$ for PDA-NFL chip and $\Delta U_{\text{IPD52 for 10 kPa}}/\Delta U_{\text{noise IPD52 for 10 kPa}} = 87.9 \cdot 10^3 / 2.5 \approx 3.5 \cdot 10^4$ for IPD52 chip. Specifications for PS module consider the values of TCZ and TCS in the temperature subranges from +5 to +25 °C and from +25 to +45 °C. The values of THZ and THS in the temperature subranges from -55 to +25 °C and from +25 to +55 °C. An example of the dependence of output signal on temperature in a range wider than the operating one from -30 to +60 ° C is shown on Fig. 9b.



a) b)

Figure 9. The output characteristics for zero output signal of ultra-highly sensitive small-sized PDA-NFL chip for 10 kPa: a) noise component, b) temperature dependence

The temperature characteristics of PDA-NFL chip for 10 kPa and two temperature subranges demonstrate:

1. Identical values with IPD52 chip for:
    a. THZ with an error limit up to 0.17 %;
    b. TCZ with an error limit up to 0.27 %/10 ^{0}C;
    c. TCS with an error limit up to 2.70 %/10 ^{0}C;
2. Improved values relative to IPD52 chip for THS with an error limit up to 0.19% ($THS_{IPD52} < 0.33$ %).

The burst pressure of ultra-highly sensitive small-sized PDA-NFL for 10 kPa and analogue IPD52 chip is equal $P_{burst} > 300$ kPa. The development has an advantage by achieved error from mechanical pressure overload ($P_{overload} = 60$ kPa):

1. applied pressure from the back side $dU_{overload\ PDA\text{-}NFL\ for\ 10\ kPa} = 0.013 \pm 0.013\%$ and $dU_{overload\ IPD52\ for\ 10\ kPa} = 0.038 \pm 0.036\%$.
2. applied pressure from the top side $dU_{overload\ PDA\text{-}NFL\ for\ 10\ kPa} = 0.008 \pm 0.008\%$ and $dU_{overload\ IPD52\ for\ 10\ kPa} = 0.019 \pm 0.018\%$.

The PS modules with ultra-highly sensitive small-sized PDA-NFL chip and IPD52 chip for 10 kPa demonstrate the same errors of long-term stability for zero output signal $dU_{stab} = 0.02 \pm 0.02$ % and sensitivity $d\Delta U_{stab} = 0.03 \pm 0.02\%$.

Final conclusion of the comparative analysis for PS modules with PDA-NFL chip and IPD52 chip shows that for the same pressure range 10 kPa and the supply voltage $U_{sup} = 5$ V: the development of ultra-highly sensitive small-sized PDA-NFL is able to reduce the chip area by 2.4 times, increase the sensitivity by 5.8 times, and also maintain the parameters for temperature characteristics, long-term stability and partially improve it.

5 samples of PS modules with PDA-NFL chip fully comply with the specifications of commercially produced PS modules at FSUE VNIIA. Parameters of samples is presented in table 2. The next research carried out for full construction of PS with PDA-NFL chip confirmed the possibility of using the development. Patents No. RU 195159 U1 dated June 13, 2019 and No. RU 195160 U1 dated June 13, 2019 were obtained for solutions for ultra-highly sensitive small-sized PDA-NFL. Practical significance of thesis in FSUE VNIIA is proved by documents of "Act of results implementation for intellectual activity No. T0522-05/028-2022 dated June 24, 2022 and No. T0522-05/029-2022 dated June 24, 2022 at FSUE VNIIA".

Table 2. Output characteristics of 5 samples of PS module with ultra-highly sensitive small-sized PDA-NFL for 10 kPa and the boundary values of parameters

Parameter name (U_{sup} = 5 V)	Pressure from … side	Design ation	Unit	Requi re-ments	Samples				
Old name					T01.1. 65	T01.1. 72	T01.1. 79	T01.1. 80	T01.2. 67
New name according to documentation					TDK22. 001	TDK22. 002	TDK22. 003	TDK22. 004	TDK22 .005
Sensitivity P = 10 kPa	back	ΔU_{10}	mV	> 75	546.0	537.7	509.5	463.6	397.5
	top				559.3	549.7	514.4	471.2	402.9
Nonlinearity P = 10 kPa	back	$2K_{NL}$	%	< 0.50	0.44	0.32	0.36	0.26	0.43
	top				0.30	0.22	0.47	0.21	0.17
Zero output signal	-	U_0	mV	< 15	12.91	-5.60	4.44	-13.11	-4.76
Zero signal changing after overload pressure (P_{over} = 60 kPa)	back	dU_{over}	%	< 0.10	0.015	0.003	0.001	0.003	0.025
	top				0.006	0.003	0.003	0.003	0.001
Temperature hysteresis of the zero signal in the range from -55 to +25 °C	back	THZ		< 0.30	0.02	0.08	0.14	0.07	0.09
	top				0.02	0.08	0.14	0.07	0.09
Temperature hysteresis of the zero signal in the range from +25 to +55 °C	back				0.05	0.09	0.12	0.09	0.06
	top				0.05	0.09	0.12	0.09	0.06
Temperature hysteresis of sensitivity in the range from -55 to +25 °C	back	THS			0.00	0.10	0.16	0.16	0.08
	top				0.06	0.11	0.17	0.07	0.04
Temperature hysteresis of sensitivity in the range from +25 to +55 °C	back				0.15	0.03	0.03	0.02	0.20
	top				0.06	0.03	0.03	0.06	0.20
Zero signal temperature coefficient in the range from +5 to +25 °C	back	TCZ	%/ 10 °C		0.14	0.11	0.15	0.06	0.17
	top				0.14	0.11	0.14	0.06	0.17
Zero signal temperature coefficient in the range from +25 to +45 °C	back				0.13	0.09	0.07	0.05	0.14
	top				0.13	0.09	0.07	0.05	0.13
Temperature coefficient of sensitivity in the range from +5 to +25 °C	back	TCS		< 3.5	2.17	2.24	2.34	2.21	2.16
	top				2.21	2.23	2.29	2.17	2.16
Temperature coefficient of sensitivity in the range from +25 to +45 °C	back				2.44	2.22	2.41	1.85	1.69
	top				2.66	2.59	2.11	2.04	1.71
Long-term stability of zero output signal (for 9 hours)	back	dU_{stab}	%	< 0.10	0.02	0.00	0.01	0.04	0.02
	top				0.02	0.00	0.01	0.04	0.02
Long-term stability of sensitivity (for 9 hours)	back	$d\Delta U_{stab}$			0.04	0.05	0.05	0.03	0.04
	top				0.01	0.02	0.01	0.05	0.02

Conclusion

The main scientific result of thesis was achieved. The result is the development and research of the implementation for circuit solution to increase the sensitivity and minimize the overall dimensions of piezoresistive pressure sensor chips while maintaining the input conditions for the geometry of mechanical structure, supply voltage and low errors. The original circuit solutions for pressure measurement were applied. The most efficient PDA-NFL chip uses non-deformable BjT with vertical structure npn-type (V-NPN) with eight p-type PRs located in places of maximum MS concentration with a certain polarity according to the change its resistance by the pressure.

Main theoretical results:

1. The issues of balanced achievement of sensitivity, overall dimensions and errors are considered based on actualization of considered researches for piezoresistive PS chip. The original solutions for the circuit application presented in the thesis based on the issues discussed in the review.

2. The application of piezoresistive and piezojunction effects for creation of piezoresistive PS chip is substantiated and used.

3. The theoretical model for operation of PS chip with PDA electrical circuit has been developed, which differs from the known WB circuits by the inclusion of two dBjTs and four PRs to the base and collector contacts of dBjT. Theoretically, the possibility of increasing the sensitivity by 2.2 times relative WB circuit has been proven.

4. There is developed operation model for PDA-NFL chip according to the proposed circuit solution, which differs from the known WB circuit by including a larger number of deformable PRs. The possibility of sensitivity increasing and reducing the errors in terms of temperature and noise dependence for output signal are substantiated. The possibility of sensitivity increasing by 3.9 times relative WB circuit has been theoretically proven.

Main practical results:

1. The output characteristics of developed piezoresistive PDA chip are researched in the comparative analysis relative to analogues with WB circuit for 60 kPa pressure range. The analysis confirmed the possibility of sensitivity increasing by 2.2 times while maintaining the input conditions for geometry of mechanical structure and supply voltage.

2. The output characteristics of the developed piezoresistive PDA-NFL chip are researched in the comparative analysis relative to analogs with WB circuit for 60, 160 and 600 kPa pressure ranges. The analysis confirmed the possibility of sensitivity increasing by 3.5 times while

maintaining the input conditions for geometry of mechanical structure, supply voltage and low errors; or minimization of overall dimensions by 2.4 times while maintaining sensitivity. The possibility of reducing the noise of zero output signal by 20 times and the errors of temperature characteristics by more than an order relative to the parameters of piezoresistive PDA chip has been confirmed.

3. The design of ultra-highly sensitive small-sized PDA-NFL chip is modernized with the most efficient circuit design for 10 kPa range. The relevance of PDA-NFL chip application as part of assembly structures for PS is proved.

4. Statistical analysis of the output characteristics of assembly structures with ultra-highly sensitive small-sized PDA-NFL chip confirmed the possibility of simultaneously sensitivity increasing by 5.8 times and reducing chip area by 2.4 times relative to the analog IPD52 with WB circuit for 10 kPa range and while maintaining supply voltage and low errors.

List of publications with topic of the thesis

Articles:

1. M. Basov, “High-sensitivity MEMS pressure sensor utilizing bipolar junction transistor with temperature compensation,” Sensors and Actuators A: Physical, vol. 303, 111705, 2020.
2. M. Basov, “Ultra-High Sensitivity MEMS Pressure Sensor Utilizing Bipolar Junction Transistor for Pressures Ranging from -1 to 1 kPa,” IEEE Sensors Journal, vol. 21, no. 4, pp. 4357 – 4364, 2021.
3. M. Basov, “Development of High-Sensitivity Pressure Sensor with On-chip Differential Transistor Amplifier,” J. Micromech. Microeng., vol. 30, no. 6, 065001, 2020.
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