AREA EFFICIENT DECODER AND SIMULATION STUDY USING QUANTUM DOT CELLULAR AUTOMATA

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Abstract

The progress and dominance of the microelectronics industry has been based on scaling and maintaining functionality at ever smaller scales. The resulting changes in size and package density have limitations due to the physical laws that govern the transistor paradigm. Quantum dot cellular automata (QCA) offer a solution to accomplish device functionalities at nanometer scales. This paper details QCA implementation with simulation results which intuitively prove they are much smaller than the same circuits in standard CMOS technology. The proposed area efficient decoder in this paper is optimal in terms of usage of number of quantum dot cells with a simpler clocking scheme and good performance. The field of quantum dots is relatively at its infancy with significant opportunities for future growth and real time implementations.

Keywords: Quantum cellular automata, Quantum dots, Decoder, QCADesigner

I INTRODUCTION

Quantum-dot cellular automata design is an emerging technology that exploits the quantum phenomena to bypass and supersede the CMOS technology. It is a novel way to perform functions with ultra low power consumption at higher operating speeds. This paper explains the implementation of logic circuits using QCA and proposes a new modified area efficient decoder layout. All simulations in this paper have been done using the QCADesigner tool.

II QUANTUM-DOT CELLULAR AUTOMATA

Quantum dots can be defined as nano structures created from standard semiconductor materials like Si/SiO2. The basic building element of this technology is the QCA cell structure. The cell structure is based on bi-state switching cells composed of four quantum dots charged with two extra electrons, which tend to occupy diagonal dots because of mutual repulsion. See Figure1.

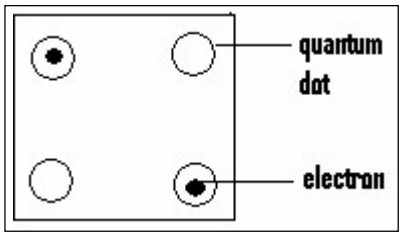

Figure1. QCA Cell Structure

Arrays of such QCA cells interact with each other and are capable of performing all logic functions equivalent to our digital design. Switching in QCA is accomplished by switching the occupancy of the two electrons. Signals propagate through the array of QCA cells as a result of interaction between the adjacent cells.

The layout of the circuit determines the interaction of the cells and hence the functionality of the overall design. The power consumption of QCA is low since only two electrons are moving. Most of the power required by QCA circuits will be used by the clocking scheme which is critical. It has been proved that any QCA circuit can be implemented in four clocking zones each Π/2 degrees [2] out of phase. See Figure2.

III QCA Logic Implementation

QCADesigner a design and layout tool has been used to implement the digital logic circuits discussed in the following sections. Computation with QCA is accomplished by designing layouts which exhibit the desired interaction of states. See Figure3 for the binary encoding of the Quantum cell states.

The first step to implement digital logic is to ensure the availability of a universally complete logic set a combination of which can realize any Boolean function – AND, OR, NOT gates.

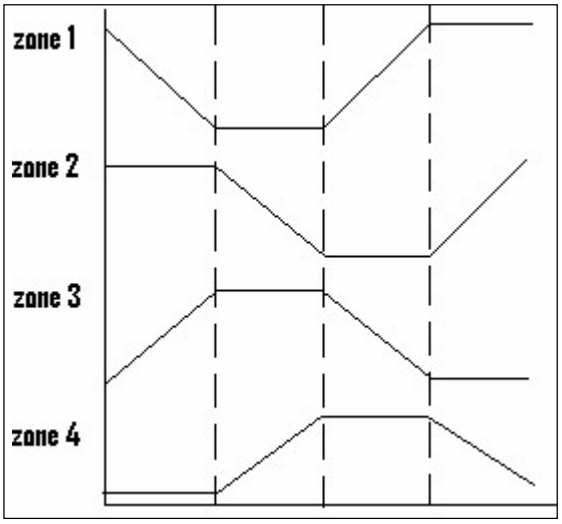

Figure2. QCA Clocking zones

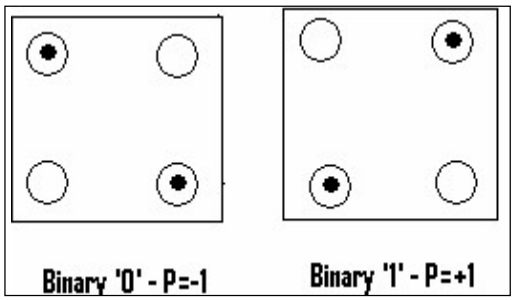

Figure3. Binary Encoding of the states

The fundamental logic gate in QCAD is the majority gate. The output of this gate will polarize to the majority polarization of the inputs. See Figure4.

$$M(A, B, C) = AB+BC+CA$$

AND and OR gates are derived from this majority gate by fixing one of the majority gate inputs to 0 (P=-1) and to 1 (P=+1) respectively.

$$M(A, B, 0) = AB$$
$$M(A, B, 1) = A+B$$

A NOT gate is implemented as shown in Figure5. If we place two cells at 45 degrees with respect to each other they will interact inversely.

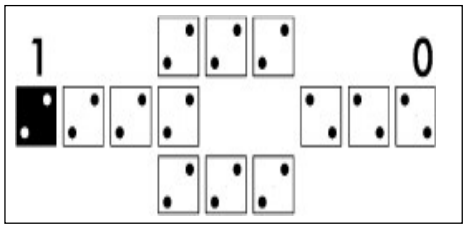

Figure5. Inverter

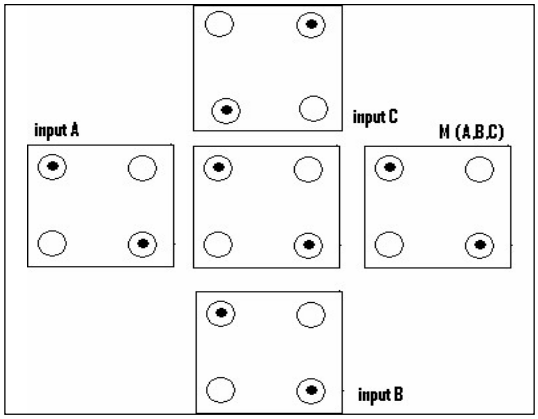

Figure4. Majority Gate

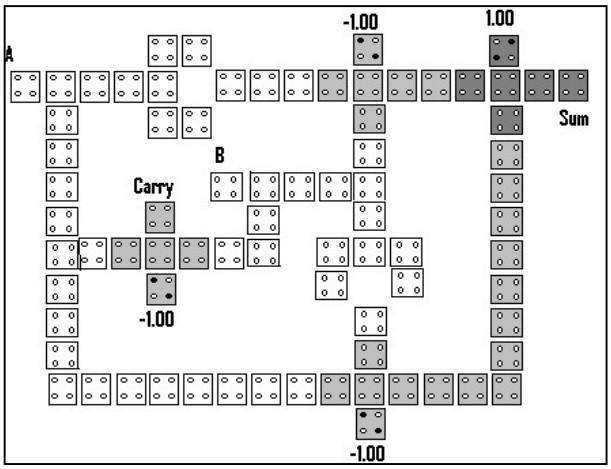

Figure6. Layout of Half Adder Circuit

A Half adder design layout and simulation result is shown in Figure7. The number of cells used in the design is 77 and the area of the circuit is 0.11um^2. This circuit uses three clocking zones for its functional implementation.

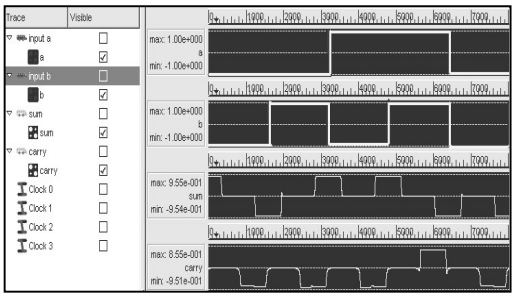

Figure7. Simulation of Half Adder

IV DECODER IMPLEMENTATION

The layout of the existing decoder implemented in [3] is shown in Figure8. It uses 164 cells and all the four clocking zones. The proposed area efficient decoder layout design is shown in Figure9. The two control lines A and B

run as inversion chains and signals are tapped off at appropriate spots decoder1, decoder2, decoder3 and decoder4 to obtain the required logic

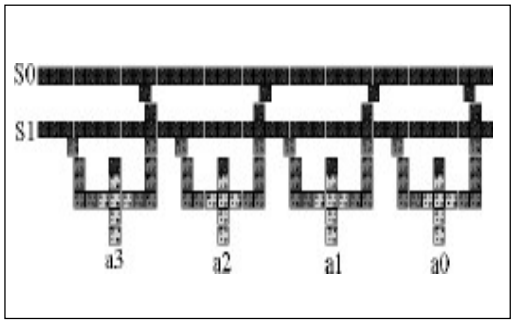

Figure8. Decoder Circuit as in [3]

This design is optimal in usage of quantum dot cells and has a simpler clocking scheme. While the decoder in [3] uses four clocking zones the proposed decoder uses only two clocking zones indicated by different shades in the Figure. The simulation result for this decoder is shown in Figure10.

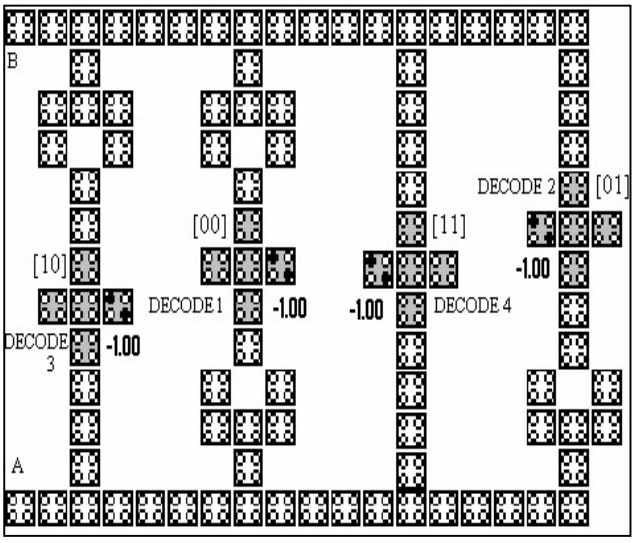

Figure9. Decoder Implementation – Design Layout

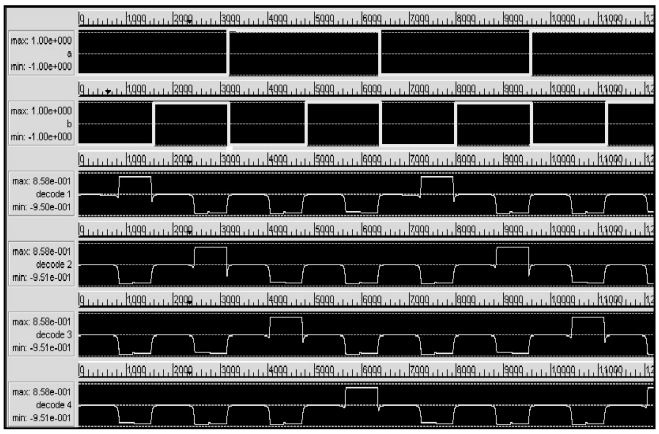

Figure10. Simulation Results for Decoder

V CONCLUSION

QCA Design has a long way to go before we can make the claim that it surpasses the present day microelectronics in all spheres of performance. This paper discusses QCA design and gives a brief description about switching, clocking and logic implementations in this technology. We see that QCA layouts are significantly smaller and easier to implement when compared to certain CMOS analogy. Further an area efficient decoder is proposed which uses a simpler clocking scheme with no compromise on performance and functionality. The design has been simulated and verified using the QCADesigner tool. The decoder discussed in this paper occupies 70% lesser area than the layout in [3]. The final results are tabulated in Table1. This is a field of great interest and recent curiosity with significant avenues for potential research implications in the near future.

Design	Area	Number of QCA cells	Clocking
Decoder in [3]	0.20 um^2	164	More complex
Proposed Decoder	0.14 u m^2	100	Simpler

Table1. Comparison of Results

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