Design of Carry Select Adder using Binary to Excess-3 Converter in VHDL

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Abstract: This paper presents a modified design of Area-Efficient Low power Carry Select Adder (CSLA) Circuit. In digital adders, the speed of addition is limited by the time required to transmit a carry through the adder. Carry select adder processors and systems. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries.

Index terms: Area-efficient, Low power, CSLA, Binary to excess one converter, Multiplexer.

I. INTRODUCTION

Today, conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path.
However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure. The basic idea of the proposed work is by using n-bit binary to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure.

II. DELAY AND AREA EVALUATION OF THE BASIC ADDER BLOCKS

Excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block.

Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

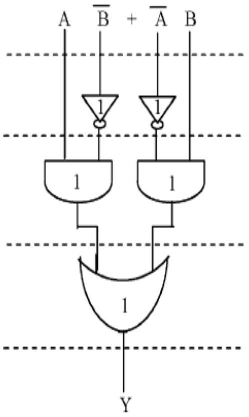


Figure 1: Delay and Area evaluation of an XOR gate.

Table 1
Delay and Area Evaluation of the Basic Blocks of CSLA

Basic Blocks	Delay	Area
XOR	3	5
2:1 MUX	3	4
Half Adder	3	6
Full Adder	6	13

III. BASIC STRUCTURE OF BEC LOGIC

Conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-bit BEC are shown in Figure.2 and Table .2, respectively.

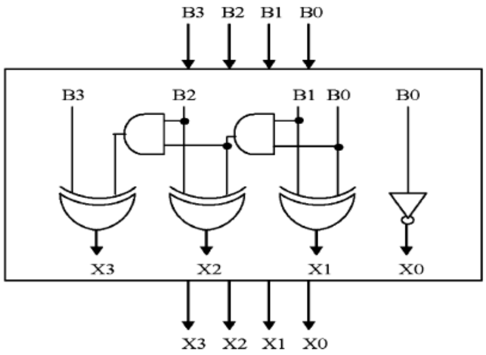
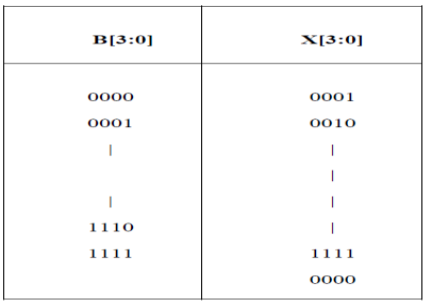


Figure 2: 4-Bit BEC

The Boolean expressions of the 4-bit BEC are

X0 = ~B0 (1)
X1 = B0^B1 (2)
X2 = B2^ (B0 & B1) (3)
X3 = B3^ (B0 & B1 & B2) (4)

Table.2 Function table of the 4-bit BEC



B[3:0]	X[3:0]
0000	0001
0001	0010
|	|
	|
|	|
1110	|
1111	1111
	0000

IV. BASIC STRUCTURE OF REGULAR 16-BIT CSLA

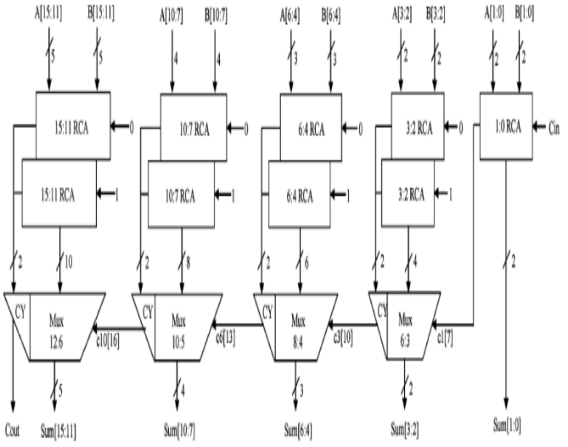


Figure 3: Regular CSLA circuit

The structure of the 16-b regular SQRT CS conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder
{c6, sum [6:4]} = c3 [t=10] +mux (5)
{c10, sum [10:7]} = c6 [t=13] +mux (6)
{Cout, sum [15:11]}=c10 [t=16] +mux. (7)

3) The one set of 2-b RCA in group2 has 2 FA for Cin=1 and the other set has 1 FA and 1 HA for Cin=0. Based on the area count of Table I, the total number of gate counts in group2 is determined as follows:

Gate Count = 57 (FA+HA+MUX) (8)
FA=39(3*13) (9)
HA=6(1*6) (10)
MUX=12(3*4) (11)

4) Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in Table 3.

Table 3 comparison parameter

Group	Delay	Area
2	11	57
3	13	87
4	16	117
5	19	147

V. DELAY AND AREA EVALUATION OF CSLA USING BEC CONVERTER

The structure of the proposed 16-b SQRT CSLA using BEC for RCA with Cin=1 to optimize the area and power is shown in Fig. 4. We again split the structure into five groups. The steps leading to the conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path. However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder) are depending on s3and mux and partial c3 (input to mux) and mux, respectively. The sum2 depends on c1 and mux.
2) For the remaining group’s the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC’s. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.
3) The area count of group2 is determined as follows:

Gate count =43(FA+HA+MUX+BEC) (12)
FA= 13(1*13) (13)
HA=6(1*6) (14)

AND=NOT=1 (15)
XOR=10(2*5) (16)
MUX=12(3*4) (17)

4) Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table 4.

Table 4 Comparison of parameters

Group	Delay	Area
2	13	43
3	16	61
4	19	84
5	22	107

Comparing Tables 3and 4, it is clear that the proposed modified CSLA saves 113 gate areas than the regular CSLA, with only 11 increases in gate delays.

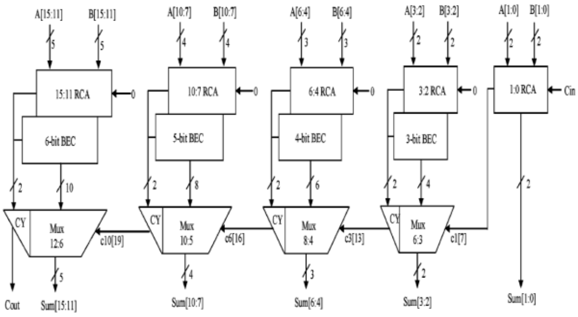


Figure 4: CSLA circuit using BEC Converter

VI. SIMULATIONS AND EXPERIMENTAL RESULTS

The proposed solutions have been designed using Xilinx.

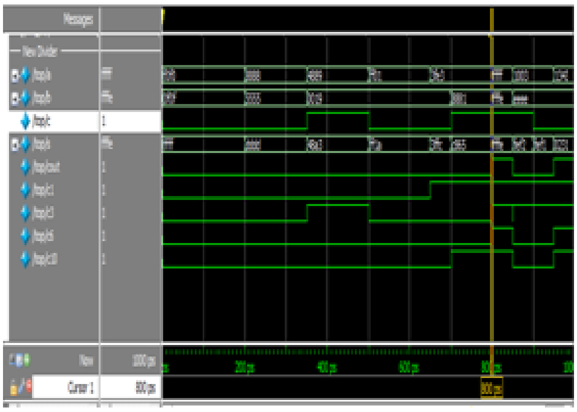


Figure 5: Simulated Results

The area-efficient carry select adder can also achieve an outstanding performance in power consumption. Power consumption can be greatly saved in our proposed area-efficient carry select adder because we only need one XOR gate and one INV gate in each summation operation as well as one AND gate and one OR gate in each carry-out operation after logic simplification and sharing partial circuit. Because of hardware sharing, we can also significantly reduce the occurring chance of glitch. Besides, the improvement of power consumption can be more obvious as the input bit number increases.

The conventional carry select adder performs better in terms of speed. The delay of our proposed design increases lightly because of logic circuit sharing sacrifices the length of parallel path.

However, the proposed area-efficient carry select adder retains partial parallel computation architecture as the conventional carry select adder design; the delay increment of the proposed design is similar to that in the conventional design as the input bit number increases. We also simulated the delay performance in the proposed area-efficient adder and conventional carry select adder with 4, 8, 16, and 32-bit respectively.

CONCLUSION

A to excess-1 code converters (BEC) to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA we can achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure.is therefore, low area, low power, simple and efficient for VLSI hardware implementation.

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