CHAPTER 1

INTRODUCTION

1.1 Introduction

The focus of this project is to design a Low Noise Amplifier (LNA) on 0.35 micron CMOS technology to meet the following specifications.

Power dissipation	10mW
Noise Figure	0.6dB
Gain	22dB
Isolation	48dB
IIP3	-5dBm
$P_{1\text{-}dB}$	-12.5dBm

Table 1-1 – Specifications that were tried to be matched in the project

1.2 Objectives:

The following five objectives were established at the outset of the project:

i) To develop a circuit topology and to size all circuit components to meet specifications; to build the LNA using 0.35 μm CMOS technology.

ii) To gain experience working with Microwind layout tool and the various types of analysis, and also study the effects of parasitic capacitances that arise out of the layout.

iii) To simulate the LNA operation in Microwind to generate gain, input impedance, noise, and linearity results .

iv) To learn about the circuit design and operation of components such as MOSFETs and spiral inductors and advantages of on-chip designing

v) To work collaboratively with an engineering design team, and learn the various aspects of designing components to meet the requirements of the customer.

1.3 Low Noise Amplifier

Communication Systems have become such an integral part of everyone's life - from mobile phones to accessing the INTERNET to radar applications. Digital signals are not good for long distance propagation in it's electrical form. Thus it becomes important to transform the digital waveforms into a form like optical signals or electromagnetic waves in which form it can be transmitted over long distances and an effective receiver system that can retrieve the signal back.

1.3.1 Need of a Low Noise Amplifier

The Digital processing systems require interfaces to the analog world. Prominent examples of these interfaces are the transmission media for wired or wireless communication. As wireless communication use air as the medium of transport of information the signals transmitted comes undergoes distortion under various noise sources and also gets attenuated as it propagates. These applications need LNAs in the receiver path as the input stage may get an input that is high in noise and low power input signal. If a normal amplifier is used in this stage it would amplify the noise along with the weak signal or it may even suppress the signal. Thus a specialized circuit that can remove the noise and add little noise on it's own it needed. This is where an LNA is needed in the field of communication.

1.3.2 What is a Low Noise Amplifier?

The Low Noise Amplifier is a special type of electronic amplifier used in communication systems which amplifies very weak signals captured by an antenna.

1.3.3 LNA in RF communication:

A low noise amplifier (LNA) is utilized in various aspects of wireless communications, including wireless LANs, cellular communications, and satellite communications. A typical receiver for a radio frequency signal (RF signal) comprises a combination of an amplifier and a mixer for signal amplification and frequency conversion. The amplifier, usually a low-noise amplifier (LNA), receives the RF signal, amplifies the RF signal and feeds the amplified RF signal to the mixer which in addition receives a local

signal from a local oscillator (LO). A critical building block in a radio receiver is the low noise amplifier (LNA). The LNA amplifies the received signal and boosts its power above the noise level produced by subsequent circuits. An LNA provides a steady gain over a specified frequency bandwidth. One common application is the use of a LNA as the input stage of a receiving circuit, such as in a mobile communication device. In a radio frequency (RF) signal receiving apparatus such as a cellular phone and a base station of a wireless communication system, a received signal has very weak intensity and includes considerable noise mixed therein. As such, the performance of the LNA greatly affects the sensitivity of the radio receiver. The low noise amplifier is capable of decreasing most of the incoming noise and amplifying a desired signal within a certain frequency range to increase the signal to noise ratio (SNR) of the communication system and improve the quality of received signal as well. Depending on signal frequency, an LNA can be implemented as an open loop or closed-loop amplifier and may also have a requirement to match a specific source impedance.

1.3.4 Criteria needed for a good LNA design:

The LNA in a circuit needs to make sure that the signal is amplified to such a level that makes further signal processing is insensitive to noise. An LNA's main performance challenge is to deliver the undistorted but amplified signal to further signal-processing units without adding noise to the signal. So one of the criterion for a circuit to act as a LNA is that it should have good amplification and also good filtering out of the signal and removing the noise. It is to be noted that an LNA is first component on the receiver side of the circuit after the antenna and hence another important parameter of consideration is that a LNA should have an input impedance of 50 ohms(impedance of an antenna). Also an LNA should have high output impedance for the further signal processing stages. So the desirable criteria for a LNA circuit can be summed up as:

- High Gain
- Low Feedback
- A low input impedance (50 ohms – as an LNA follows an Antenna at the receiver side)
- High Output Impedance
- Linearity
- High Noise Figure

These properties determines the operational quality of an LNA.

1.3.5 Factors to be considered in the design of a LNA:

The LNA's operating frequency and, in some cases, its operation bandwidth affect the maximum achievable performance. Furthermore, to meet the specifications of many applications, designers must consider its nonlinearity. But different systems often have diverging requirements. On the one hand, high-performance wired applications need a very high bandwidth, which necessarily increases power consumption. Power consumption, on the other hand, is especially relevant for low-bandwidth wireless applications. For high-bandwidth systems, bandwidth may be more important than linearity in LNA performance, but we want to avoid contradictory design constraints. Also an important factor in the design of LNA is the surroundings in which the circuit may be operated in and the nature of the transmission of data. Therefore, the design and selection of an LNA boils down to the type of application it is used in and the nature of the surroundings.

1.3.6 Applications of LNA:

LNA applications include communication products using the code division multiple- access, Global Positioning System, Global System for Mobile Communications, Universal Mobile Telecommunications System, Blue-tooth, and other wireless standards. These applications operate in a wide variety of frequency bands.

1.4 Microwind Layout Tool:

Microwind is an integrated chip layout and simulation package written as an aid for learning sub-micron Complementary Metal Oxide Semiconductor (CMOS) integrated circuit design and it has many features that make it unique. Microwind combines various computer tools in a single package that allow the user to layout, check and simulate a CMOS circuit interactively. It also has a compiler that can create the Layout of a logic gate directly from a boolean expression.

The biggest advantage of Microwind is that it is a Free-ware for academic purposes. The Microwind tool has a unique property that it generates the parasitic capacitances that follow the layout area. This unique feature of Microwind allows us to explore the in-depth details of layout designing and the also gives us a better understanding into what actually happens in the world of fabrication of an IC. An IC when fabricated may not match the exact operation of the circuit as per it's design. This may be due to the various parasitics, some significant and some negligible. The understanding of how and where parasitic capacitances can influence the circuit operation is an important understanding acquired in the course of the project.

Microwind also has additional capabilities which include 2-dimensional cross-sectional view of the circuit and a 3-dimensional view of the fabricated IC. These interactive features make Microwind attractive and easy to understand.

1.4.1 Process Technologies in Microwind:

Microwind has been structured in a manner that allows different processes to be accessed and studied. This is accomplished using the selection of boundary for a design. In semiconductor terms a foundry is the central chip-fabrication plant that accepts designs from the outside world and uses the design files to manufacture chips. Foundries characterize different process lines by the minimum allowed feature size. Microwind has range of foundry options that can be used to design circuits in different feature size technologies. These technology files are saved with a '.rul' extension.

1.4.2 Microwind Netlist:

Microwind provides for the extraction of the netlist of the circuit which contains all the components of the circuit and and the MOSFET parameters and mostly importantly gives us the details of the parasitic capacitances that Microwind computes for the layout. The netlist is saved with the extension as '.cir' and the name as that of the MSK file. The layout gives a detailed parametric view of the circuit that can be exported in P spice or Winspice formats. The study of the netlist gives a better understanding of the circuit.

1.4.3 Microwind DAT Files:

Microwind outputs the data of a simulation as '.dat' files that can be opened using notepad and it contains the simulation values. This software does not provide the extraction into excel files and the only was to access the simulation results is using the DAT files. The values can be taken out of the notepad and copied for mathematical calculations.

1.4.3 Microwind MOS Layout Generator:

The MOS layout generator provides a simple way to create transistors with specific length (L) and width(W) values. The MOS generator windows gives the option of entering the dimensions in microns or in terms of lambda. This window also gives the option to select a NMOS or a PMOS or a double gate and belonging to low-leakage, high-power or high-speed type depending on the technology that the window is in. Along with the above options it also provides for specifying the number of fingers as in the case for multi-finger MOSFET design.

The software uses the BSIM4 platform in a simplified version to make the simulation faster. This represents a considerable constraint when it comes to modeling of the BSIM parameters to suit the design specifications. The advantages of the software overweight it's disadvantages.

CHAPTER 2

REVIEW OF RELATED LITERATURE

In section I review the various concepts and papers that have helped me achieve my results in the course of the work.

2.1 Miller effect:

The Miller effect accounts for the increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of the effect of capacitance between the input and output terminals. Gate-to-drain capacitance, C_{gd}, is a nonlinear function of voltage and is the most important parameter because it provides a feedback loop between the output and the input of the circuit. Since the gate-source voltage increases and the drain-source voltage decreases during the turn-on transition, Miller's effect is significant, by increasing the transistor input capacitance, the gate drive and drive power requirements, reducing the switching C_{gd} is also called t speed. The Miller capacitance is to be avoided because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances. Charge time for the Miller capacitance is larger than that for the gate to source capacitance C_{gs} due to the rapidly changing drain voltage.

2.2 BSIM4 parameters:

Analytical models are limited in their ability to accurately predict the behavior of MOSFETs under time-varying conditions. Microwind uses a simplified BSIM4 equation set to allow fast simulations. BSIM stands for Berkeley Short-Channel IGFET Model. The full BSIM4 description uses around 200 parameters; the Microwind implementation is based on 20 of the most important values. It is important to note here that this very limitation in the number of parameters used represents a constraint in the MOSFET modeling as only these parameters are rendered to change.

BSIM (Berkeley Short-channel IGFET Model) refers to a family of MOSFET transistor models for integrated circuit design. Accurate transistor models are needed for electronic circuit simulation, which in turn is needed for integrated circuit design. As the devices become smaller each process generation (see Moore's law), new models are needed to accurately reflect the transistor's behavior.

The following table contains a set of the Microwind BSIM4 parameters.

Parameter	Definition
VTO	Long-Channel threshold voltage
VFB	Flat-band Voltage
TOX	Oxide Thickness
K2	2nd order body bias factor
DVT0	1st order short channel factor
DVT1	2nd order short channel factor
LPE0	Lateral non-uniform doping parameter
ETA0	DIBL coefficient
NFAC	Sub-threshold turn-on factor
U0	Low field mobility
UA	Vertical field mobility factor
UC	Body-bias mobility factor
PSCBE1	1st substrate induced body bias factor
PSCBE2	2nd substrate induced body bias factor
VSAT	Saturation velocity
WINT	Channel width offset parameter
LINT	Channel length offset parameter
KT1	Temperature coefficient(V_T)
UTE	Temperature coefficient
VOFF	Sub threshold offset voltage
PCLM	Channel length modulation parameter

Table 2-1 – showing the Microwind BSIM4 Parameter

2.3 Modeling and performance of Spiral Inductors:

The modeling and performance of spiral inductors were studied in detail and the advantages were understood by making use of the IEEE publication - “Modeling and performance of Spiral Inductors in SOI CMOS Technology”[2] the various parameters in the analysis of the spiral inductor were understood and it's equivalent circuit studied.

2.4 Reference Low Noise Amplifier Design for 0.35micron technology

The reference circuit and the specifications for the LNA was based on the paper “A Low-Power Low-Noise Amplifier in 0.35-µm SOI CMOS Technology”[1] and the requirements and the impedance matching techniques were studied in detail. This paper provided with a road-map for the LNA design and the project tried to achieve the results of the paper as close as possible.

CHAPTER 3

METHODS AND PROCEDURE

Basic MOS amplifiers are the main building blocks of a vast array of analog signal processing systems as well as other analog electronic circuits. The overall performance of a complex circuit strongly depends on the performances of its basic building blocks. MOSFET amplifiers are also reputed for their higher slew rate than other designs such as the bipolar designs. MOSFET amplifier designs are stable thermally, requiring no more circuitry, without any chance of thermal runaway.

Low Noise Amplifier Design:

The low noise amplifier designs are to be characterized in such a way that the circuit is poised to have a low input impedance, high output impedance and also low feedback in the circuit. In this context we examine the advantage of a cascode amplifier over a single stage amplifiers.

3.1 Cascode Configuration:

The cascode is a two-stage amplifier composed of a transconductance amplifier followed by a current buffer. In modern circuits, the cascode is often constructed from two transistors with one operating as a common emitter or common source and the other as a common base or common gate. The circuit in this work is a pair of common base and followed by common gate. The cascode improves input-output isolation (or reverse transmission) as there is no direct coupling from the output to input. This eliminates the Miller effect and thus contributes to a much higher bandwidth.

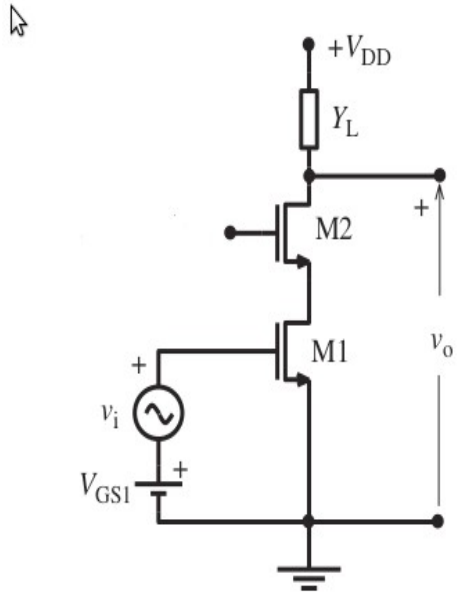


Figure 3.1 – Showing a general cascode amplifier

The major advantage of the Cascode circuit arrangement (as shown in the figure – 3.1) comes from the placement of the upper MOSFET as the load of the input (lower) MOSFET's output terminal (drain). Because at operating frequencies the upper MOSFET's gate is effectively grounded, the upper MOSFET's source voltage (and therefore the input transistor's drain) is held at nearly constant voltage during operation. Thus the upper MOSFET exhibits a low input resistance to the lower MOSFET, making the voltage gain of the lower MOSFET very small, which dramatically reduces the Miller feedback capacitance from the lower MOSFET's drain to gate. This loss of voltage gain is recovered by the upper MOSFET. Thus, the upper transistor permits the lower MOSFET to operate with minimum negative (Miller) feedback, improving its bandwidth.

If the upper MOSFET stage were operated alone using its source as input node (i.e. common-gate (CG) configuration), it would have good voltage gain and wide bandwidth. However, its low input impedance would limit its usefulness to very low impedance voltage drivers. Adding the lower MOSFET results in a high input impedance, allowing the cascode stage to be driven by a high impedance source.

If one were to replace the upper MOSFET with a typical inductive/resistive load, and take the output from the input transistor's drain , the Common - Source configuration would offer the same input impedance as the cascode, but the cascode configuration would offer a potentially greater gain and much greater bandwidth. The cascode arrangement is also very stable. Its output is effectively isolated from the input both electrically and physically.

The cascode arrangement offers high gain, high bandwidth, high slew rate, high stability, and high input impedance. It requires two transistors and requires a relatively high supply voltage. For the two - MOSFET cascode, both transistors must be biased with ample V_{DS} in operation, imposing a lower limit on the supply voltage.

3.1.1 Comparison of Single Stage and Cascode Amplifiers:

The Cascode amplifier as discussed in the previous section has a number of advantages over the single stage amplifier which includes better gains, better bandwidth, reduced Miller effects and others. The single stage and cascode amplifier models were examined and compared.

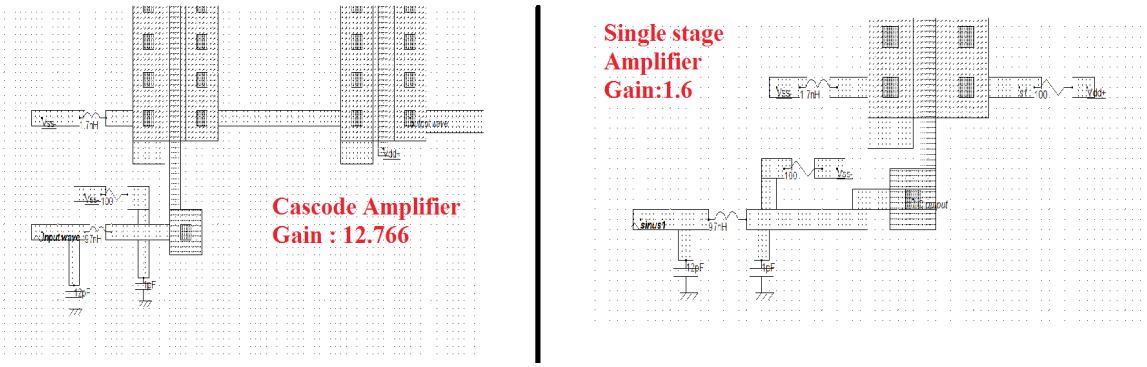


Figure 3.2 – Showing the layouts of the single stage and cascode amplifier and their gain

It was observed that the gain of a single stage amplifier was very less when compared to the high gain of the cascode amplifier. This high gain can be attributed to the efficiency in the Cascode model of the circuit.

3.2 MOSFET Modeling:

MOSFET is an acronym for Metal Oxide Semiconductor Field Effect Transistors. It is the smallest switching element that can be used on a mass-produced integrated circuit. A MOSFET is a 3-dimensional structure built by sandwiching patterned regions of three materials – poly-gate, gate oxide and semiconductor that are fabricated directly in the silicon.

Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals, the body (or substrate) of the MOSFET often is connected to the source terminal, making it a three-terminal device like other field-effect transistors. When two terminals are connected to each other (short-circuited) only three terminals appear in electrical diagrams. The MOSFET is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common.

MOSFETs are broken down into two types depletion type and enhancement type . In enhancement mode MOSFETs, a voltage drop across the oxide induces a conducting channel between the source and drain contacts via the field effect. The term "enhancement mode" refers to the increase of conductivity with increase in oxide field that adds carriers to the channel, also referred to as the inversion layer. In the less common depletion mode MOSFET, the channel consists of carriers in a surface impurity layer of opposite type to the substrate, and conductivity is decreased by application of a field that depletes carriers from this surface layer.

They are again broken down based on their polarities – 2 types of MOSFETs found. An n-channel MOSFET conducts electrical currents using negatively charged electrons. These are called nMOS transistors or nFETs. A p-channel MOSFET is exactly the opposite as it conducts electrical current using positively charged particles called holes. These are called pFETs or pMOS transistors.

Microwind offers a in-built MOS generator that generates the MOSFET models for a given input width and length with various options such as low-leakage based on the technology.

3.2.1 N-Channel MOSFET analysis:

An N-channel MOSFET is one in which the electric current is due to the electrons that flow from the n-doped source terminal to the drain terminal. N-type MOSFETs are built on ptype substrate which is usually a silicon crystal lightly doped with boron. The central region of the NMOS has the gate terminal which acts as control electrode for the device. The voltage on the gate determines the ability of the NMOS to conduct an electric current between the two separated 'n^{+}' regions in the silicon. An 'n^{+}' region is one where we have an excess of negatively charged electrons to carry a current. A gate oxide layer is formed between the poly-gate and the silicon layer forming an insulating layer between the conducting poly gate and the p-substrate as shown in the figure 3.1

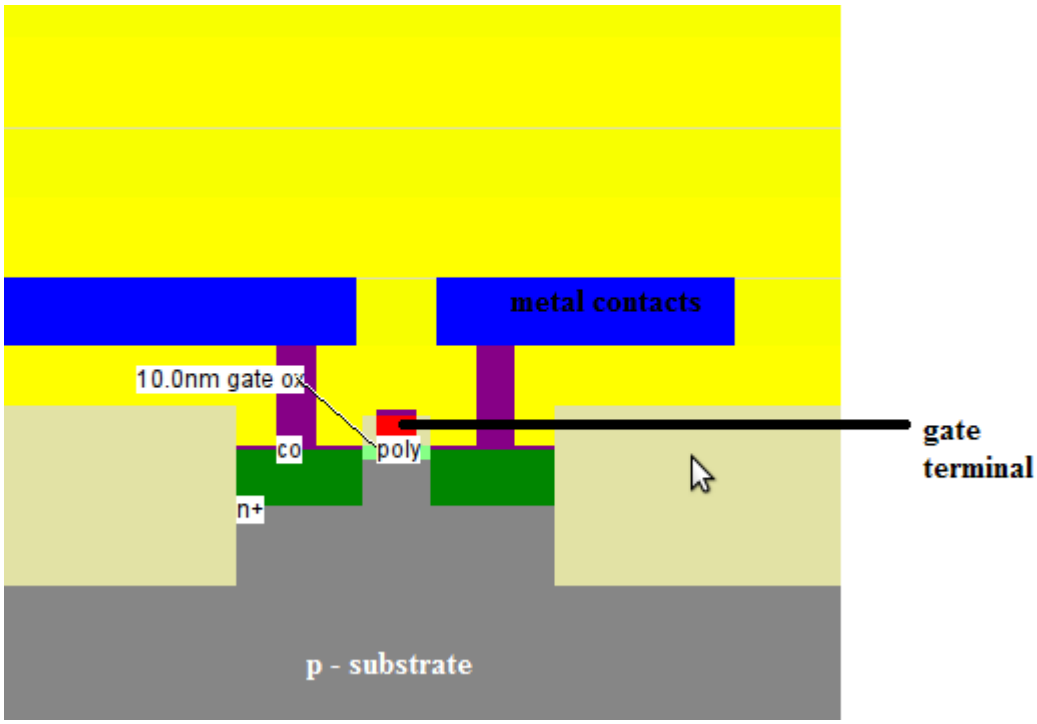


Figure 3.3 – Showing 2-dimensional cross-sectional view of an NMOS

Electrical Properties of NMOS:

The Threshold voltage of a MOSFET is defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor or to observe the minimum voltage required to switch on the Transistor. This threshold voltage is a positive value for an NMOS. The NMOS conducts

currents above this threshold voltage. It is thus important to note that when using a MOSFET as an amplifier we have to make sure that the MOSFET is operated in the linear region by giving a proper biasing potential.

Parasitic Capacitances:

The Microwind layout tool assigns parasitic capacitances to the MOSFET model which has been pointed out in following figure- 2. These parasitic capacitances are assigned values depending on the Rule file (process technology file) about which, has been discussed in the later sections.

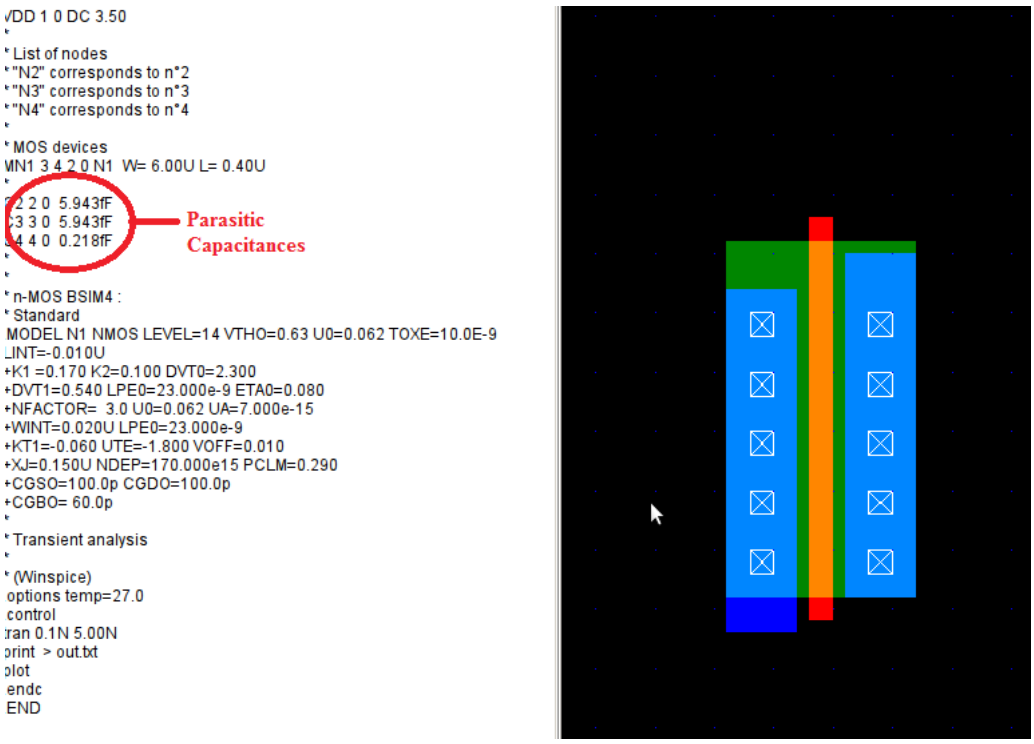


Figure 3.4 – Showing a layout of an NMOS with the parasitic capacitance as generated by Microwind

The Microwind Layout tool also produces a 3-dimensional view from the fabrication point of view as shown in the following figure.

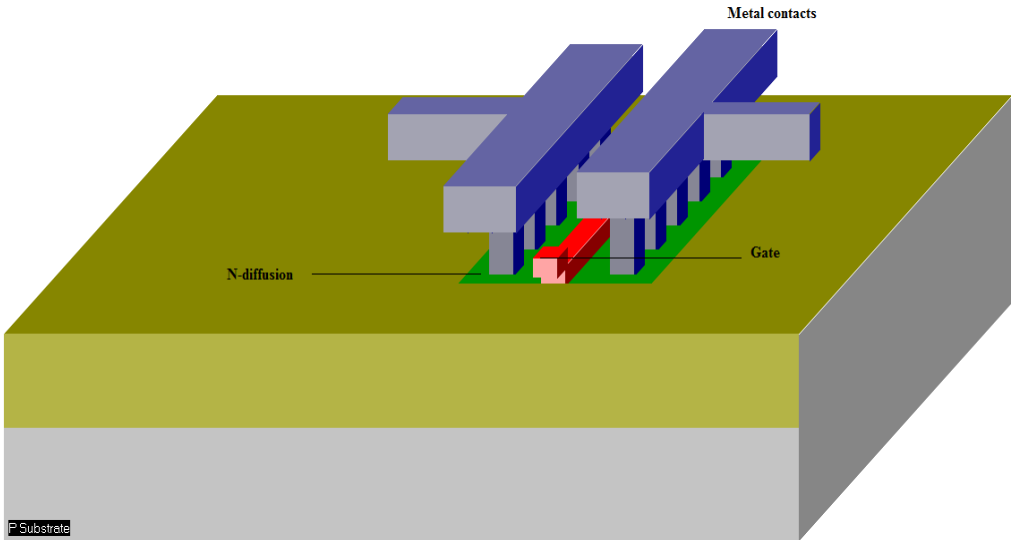


Figure 3.5 – Showing the three dimensional view of an NMOS as generated by Microwind

3.2.2 P-Channel MOSFET analysis:

A P-cahnnel MOSFET is similar to the NMOS with the regions reversed. The PMOS in Microwind is built by constructing an N-well on a P-substrate, the left and right side of the device are p^+ regions indicating an excess positive charge. The P-doped drain and source mean that the current flow is due to the holes and not the electrons as in case of the NMOS.

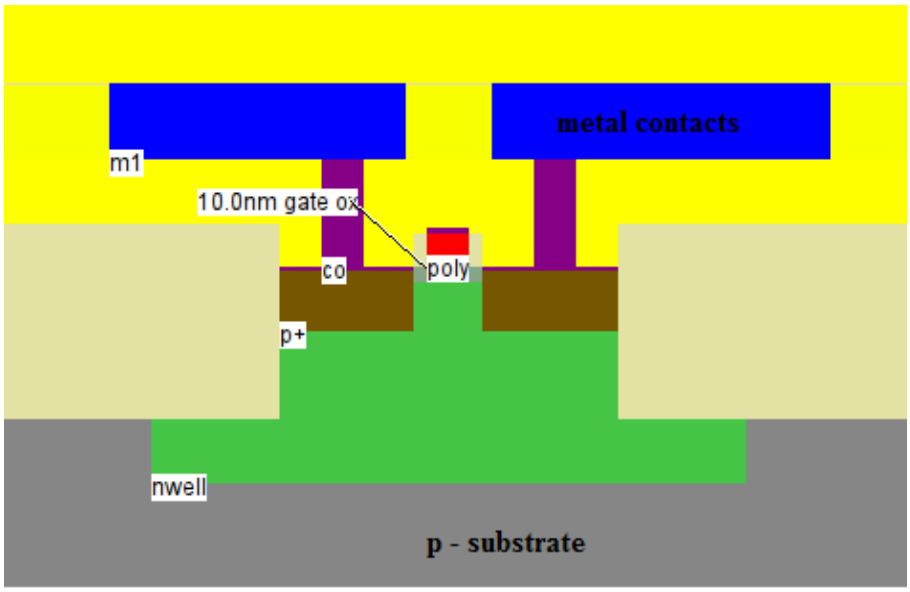


Figure 3.6 – showing the 2-dimensional cross sectional view of a P-type MOSFET

Electrical Properties:

The electrical properties of a PMOS are similar to the point that a threshold voltage has to be applied for the PMOS to conduct but it differs from the NMOS in the voltage value, which for a PMOS is negative and it conducts for negative voltages less than the threshold voltage, at the gate. It is also to be noted that the majority charge carriers are the holes and not the electron and thus are generally considered slower than NMOS.

Parasitic Capacitance:

Microwind as in the case of the NMOS generates parasitic capacitances for the PMOS also which is dependent on it's geometry.

3.2.3 Multi-finger MOSFET Design:

MOSFETs with large dimensions are generally used in analog CMOS circuits and multiple-finger parallel devices is the most common method in such applications. This method of implementation involves the implementation of a single wide FET in into FETs of smaller widths sharing the common gate terminal. This implementation as shown in the figure- is equivalent to a single FET of dimension of - number of fingers x width of each finger. A multi-fingered MOSFET design implementation in Microwind is as shown in the following figure-

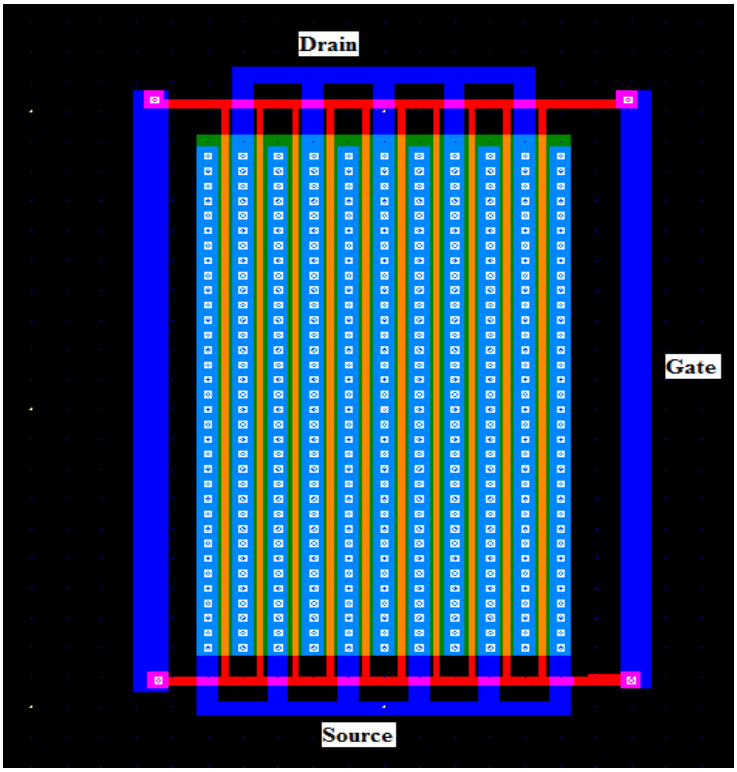


Figure 3.7 – Showing the layout of a multi-finger MOSFET

In order to avoid using transistors with gate widths of up to 350 μm, a technique known as gate splitting was used. By placing multiple devices in series, the gate width was split into smaller units known as fingers. The use of fingers allowed for smaller devices to be used, which optimized the total area occupied by the LNA circuit. With fingers, the correct gate width was still achieved, but with the essential benefit of a more compact design. For the LNA design, the ransistors were set up to have ten fingers each, resulting in ten smaller transistors with widths of 35 μm each .

Because fingers were used to place multiple devices in series to achieve the total width of a single transistor, the resulting transistor needed to be connected properly. Having multiple fingers essentially broke the total transistor up into smaller sections. Therefore, each of these smaller sections needed to be tied together. The gates, drains, and sources of each finger were tied together using the same material from which it was created.

A careful implementation of a multi-finger MOSFET was done and an important observation was made that the parasitic capacitances of a multi-finger MOSFET for a particular dimension is less than that for the same dimension implementation of a large transistor. This is shown in the net-lists of both the transistors in the figure- , shown below.

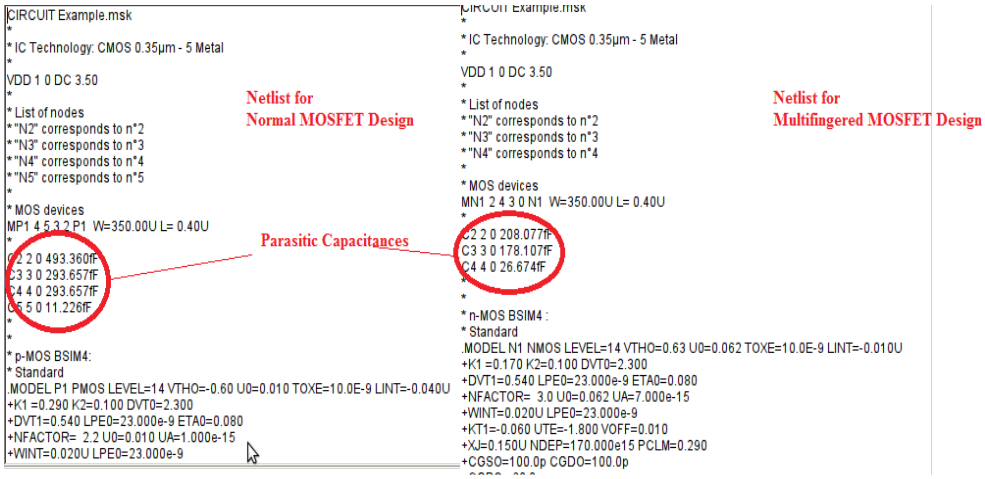


Figure 3.8 - Showing the lower parasitic capacitances for the multi-finger MOSFET implementation

3.2.4 Final MOSFET Model:

The operation of a MOSFET is dependent on the various parameters of the circuit it is used in. This means it is dependent on the technology it is designed in, the various parameters including the stack height dictates the parasitic capacitances and the gain of the circuit. Unfortunately not much is known about the MOSFET design as used in the circuit except for the Width(W) and Length(L) parameters. It also doesn't provide any data on the MOSFET modeling to compare the results with and hence a MOSFET with the W and L values were selected and also the Multi-finger MOSFET was implemented.

The parameters of the MOSFET that has been implemented in the LNA circuit are:

Parameters	Value
W (width)	350 microns
L (Length)	0.40 microns
Threshold Voltage	0.63V
g_m	242 milli-mhos

Table 3-1 – showing the Parameters of the final MOSFET model

3.3 Inductor Analysis:

An Inductor is one of the most important parts of a RF circuit as the inductance value plays a major part in the tuning and filtering of noise and determines the operating frequency of such a circuit. With such importance relied on the inductor it becomes important that accurate inductor values are achieved - on chip. An on chip inductor model has an advantage over an external addition of an inductor as it ensures that an accurate inductance value can be fabricated and the operation of the circuit would be assured and maintained intact. Thus it becomes important that we have a proper model of an inductor that when constructed through fabrication can be assured to have a proper inductance value that can be calculated easily from it's geometry. There are many inductor models and of them on of the most readily used model is the spiral inductor model. The achieved LNA circuit uses the implementation of a spiral inductor model.

3.3.1 Spiral Inductor Design:

A general spiral inductor is as shown in the figure. The inductance, resistance and the metal to substrate capacitances are all depend on the geometry of the inductor and is also dependent on the type of metals used. The spiraled inductor models provide the resistance from the metal l;ayer formed which is dependent on the sheet resistance of the

metal used. The length of the metal dictates the inductance and also the gaps in the metal give rise to the mutual inductance that gives the net inductance of the whole model.

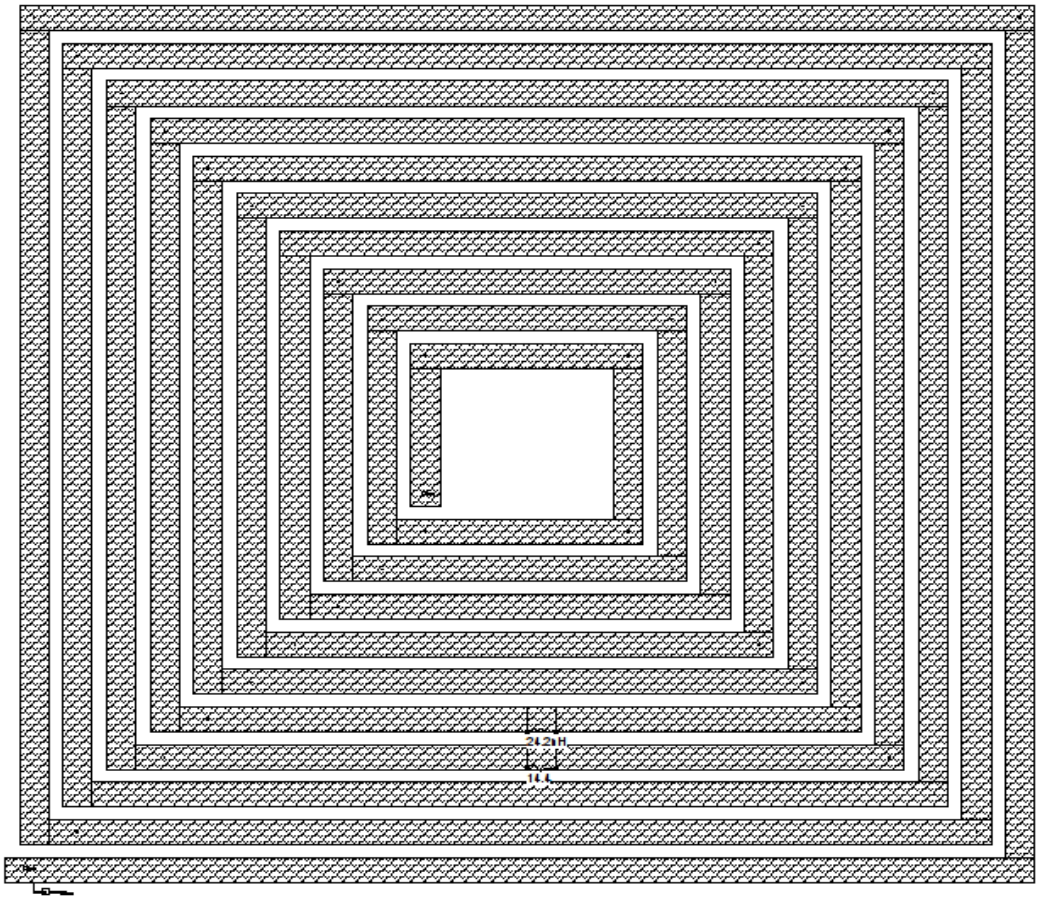


Figure 3.9 – Showing the basic Spiral Inductor layout in Microwind

Microwind offers spiral inductor implementation where in the user can modify the geometry of the spiral inductor through the 5 parameters:-

1. Metal width
2. Metal spacing
3. Number of turns
4. Hollow
5. Type of metals used.

The inductance value, it's equivalent resistance value and thus the Q- factor and it's metal to substrate capacitances are dependent on the various parameters of simulation which are a part of the BSIM4 manual. An exact match of the various parameters including frequency of operation, inductance and the Q-factor values was found to be achieved with the in-built BSIM4 parameters.

A multi-layered inductor is as shown in the figure-

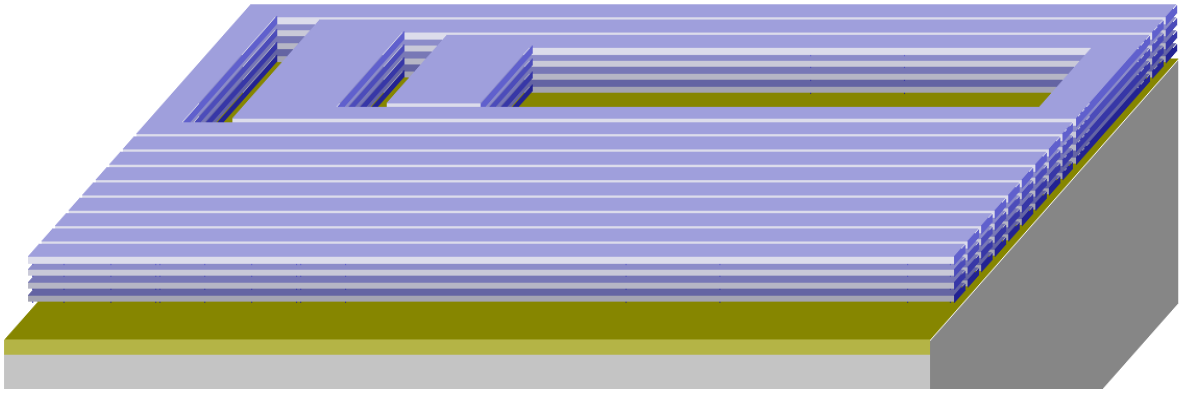


Figure 3.10 – Showing the 4-layered inductor in 3-dimensional view

3.3.2 Analysis of various Inductor Models:

A number of inductor models, using the various parameters that Microwind provides, were studied and the analysis of the various parameters involved and the frequency of operation were studied. The reference values for the inductor design from the paper were 28nH inductance, 13.8ohms series resistance and a Q-factor as high as 7.8.

An important factor that played a role in the choice of the inductor was the metal to substrate capacitance of the inductor model. The metal to substrate capacitance plays an important factor as it determines the cut-off frequency of the inductor model and acts as a kind of a filter with the capacitance. Moreover, it was found that the capacitances as generated by the inductor model are too huge to be neglected. Thus, it becomes inevitable in the context of inductor selection that a trade off be made on the inductor geometry to balance the offset in frequency due to the metal to substrate capacitance. With

this pretext in mind now we analyze the various inductor models that were implemented and tested with the circuit and the parameters that were matched.

1. A 4-metal layered inductor, made of metal-1, metal-2, metal-3 and metal-4 was found to match approximately the inductance and resistance values along with the Q-factor value. It was also noted that the metal to substrate capacitance values, as mentioned in the paper where not achieved. And also the frequency of operation of the circuit with this inductor model was found to be at 1GHz.

2.. A single metal layered inductor with the dimensions of 10 turns, 10 microns metal width and metal spacing of 5microns and hollow of 40microns was found to match the inductance value, the resistance value and also the Q-factor value. The match was achieved by changing the sheet resistance value of the metal-1 in the Rule file which is the process technology file for Microwind. But the model when implemented in the circuit was found to operate the circuit at a frequency of 696MHz.

3.An ideal inductor of 28nH was not found to produce the necessary tank effect as needed for the circuit and was not found to be suitable for the operation of the LNA as it was not able to reproduce the sine wave at the output.

4. Singe layered inductor of dimensions – 10 turns, 10micron metal width, 5micron spacing and 100microns hollow and it was found that with such a model in the circuit the peak gain frequency of the circuit was found to be at 434MHz

\

Table 3-2 – Showing a comparison of the various inductor models tested

Parameters	*4 metal layered*	*Single metal layered*	*Ideal Inductor*	*Single layered (final select)*
Inductance	Yes	Yes	Yes	No
Resistance	Yes	Yes	No	No
Q - factor	Yes	Yes	No	No
Resonant frequency	No	No	No	Yes

The final selected single layered inductor model, even though it did not match the inductance, resistance and the Q-factor values but it matched the frequency of operation of the circuit. The inductor model when implemented in the circuit, along with the parasitic capacitances generated by Microwind, make the circuit to operate with a peak gain at 435MHz. The values as advocated by the paper are difficult o be maintained as it uses a low parasitic capacitance value.

3.4 Noise Analysis:

3.4.1 Noise

In a broad sense, noise can be characterized as any undesired signal that interferes with the main signal to be processed. Even when an amplifier has no input signal, a small randomly fluctuating output signal can still be detected and is referred to as noise. Noise in electronic components is caused by random thermal fluctuations of electrons. Therefore any device operating above absolute zero will generate noise. Noise arising in an electronic component or a device is historically classified as – (1) Thermal noise (2) Shot noise (3) Flicker noise (4) Partition noise Thermal noise, also called Johnson noise occurs in any conductor due to random motion of electrons caused by thermal agitation. The shot noise is produced due to the random variations in the arrival of electrons at the output electrode of an amplifying device. For amplifying devices shot noise is inversely proportional to the transconductance of the device. In Unipolar devices like FET's, shot noise is so minimum that it can be neglected. Flicker noise is also called low frequency noise & appears at frequencies below few KHz. Flicker noise is generated due to fluctuations in the carrier density. These fluctuations in the carrier density will cause the fluctuations in the conductivity of the material. This will produce a fluctuating voltage drop when a direct current flows through a device. This fluctuating voltage is called as flicker noise voltage. Since flicker noise has a 1/f frequency spectrum with n close to unity, this noise can be neglected for microwave frequencies partition noise is is generated when the current gets divided between two or more paths. The devices like FETs, HEMTs draw almost zero gate bias current, hence keeping the partition noise to its minimum value.

The operation of a Low Noise Amplifier is to amplify the input signal which may contain large amounts of noise (as it may be contaminated as it travels through the air medium) without it itself adding much noise and also providing a good gain. The LNA model thus formed should be designed in such a way that it minimizes the amount of noise

that it generates in itself. This is achieved by careful selection of the circuit components as it is well known that an addition of a resistance, which in itself generates thermal noise, results in the circuit adding noise. Thus avoiding usage of resistances and use of reactive components in it's place can largely help in reducing the noise produced.

3.4.2 Effects of the various Components on the Noise:

The noise characteristics of a circuit boils down to the various components that are used in the circuit design. Like, when there are more resistance in the circuit the designer must be vary of the fact that it would lead to addition of thermal noise component in the circuit. When designing a circuit such as a LNA, this consideration is given more importance as the requirements of an LNA is that it should itself add as little noise as possible. Thus now let us see the effect of the various components in the circuit that affect it's noise output.

Firstly, the effect of the usage of a reactive part instead of a resistive component was carefully studied. The figure below shows the comparison of the effect of using a reactive and resistive components at the source of the MOSFET with the FFTs of the output as given from the Microwind design tool.

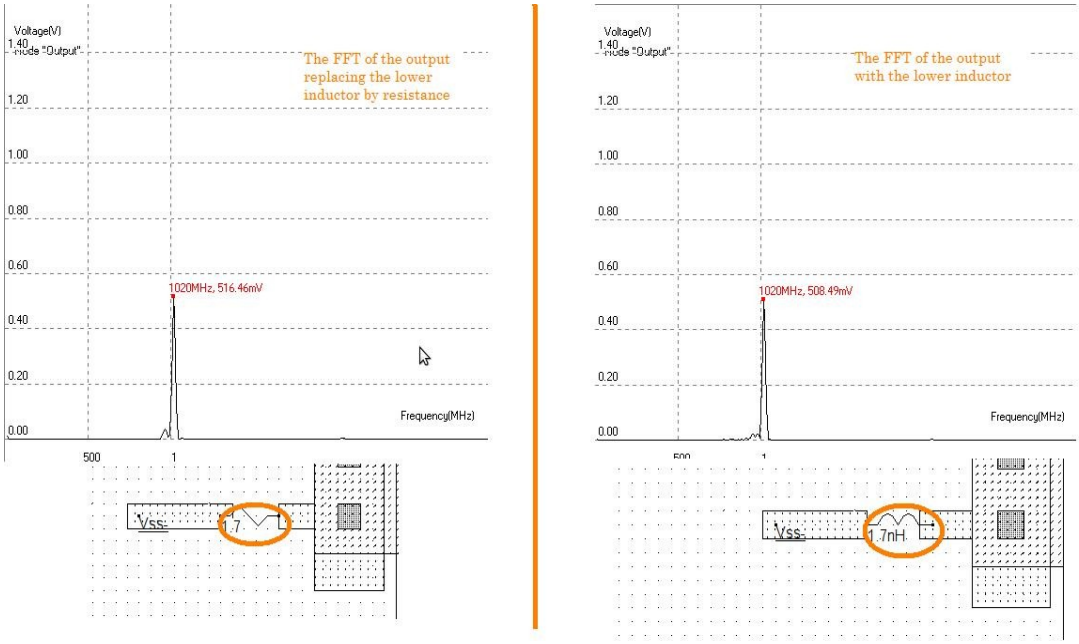


Figure 3.11 – showing the effect of replacing the inductor with a resistive component.

The above analysis was done by replacing the source to ground inductance of the circuit with a resistance and the effect is seen in the level of noise seen at the output. The replacing of the resistance, was done keeping in mind to replace the inductor with an equal impedance resistor. As clearly seen in the FFTs ,the usage of the resistance adds more noise and this can be seen with the more frequency components at the output.

Next the effect of the input capacitance network was studied. Capacitances are generally used to block the DC components as it allows the AC components. Here as the capacitances are grounded they act as ground to the high frequency components and in the absence of the capacitor these components of the noise are expected to show up at the output. Clearly the removal of the capacitance can be seen to add noise to the output which otherwise would have been filtered off. Thus we can infer that the removal of the capacitances constitute addition of noise at the output in the absence of the filtering. This is seen in the figure followed.

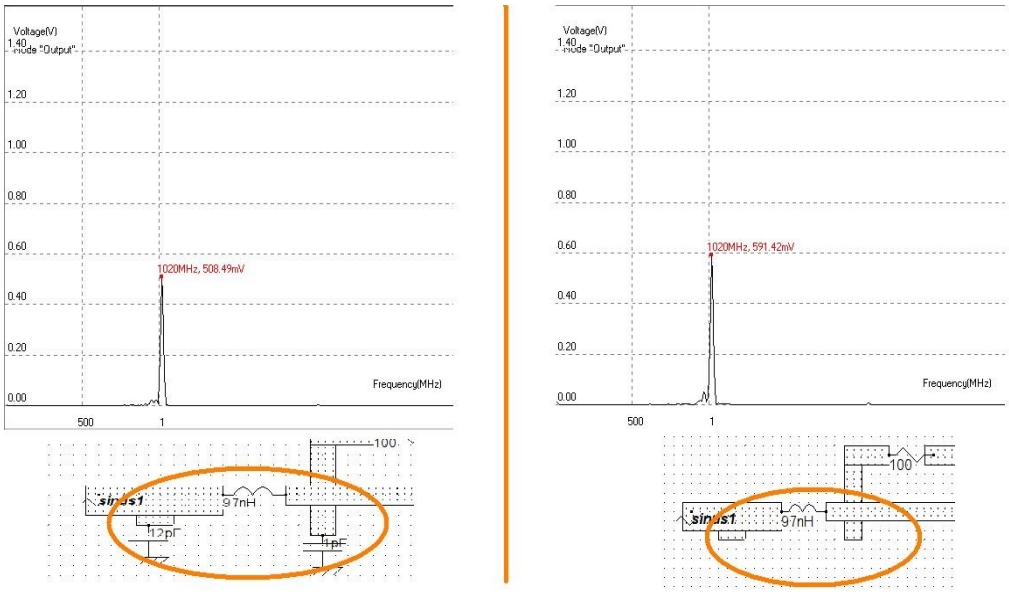


Figure 3.12 – showing the effect of eliminating the capacitances at the input stage of the circuit

Another important filtering circuitry is the formation of a frequency selective circuit that forms at the input stage with the inductor and the capacitances. This frequency selective circuit further reduces the noise into the further stages.

3.4.3 Noise Filtering Capabilities of the LNA

The noise filtering capabilities of the circuit can be illustrated by the various stages of the circuit.

➔ The input stage has an LC circuit that acts as a filtering circuit and filters out most of the noisy components. The input stage filtering removes most of the noise that has been shown in the figure – 3.11(b) . This ensures that the noise input to the MOSFET stage is significantly lower.

➔ The parasitic capacitances at the input stage of each MOSFET act as shorts for the higher frequency components that results in smoothening the wave that acts on the MOSFET gate.

➔ The output stage of the circuit has huge parasitic capacitances of the order of picofarads and this adds to further smoothening at the output resulting in reduced noise at the output.

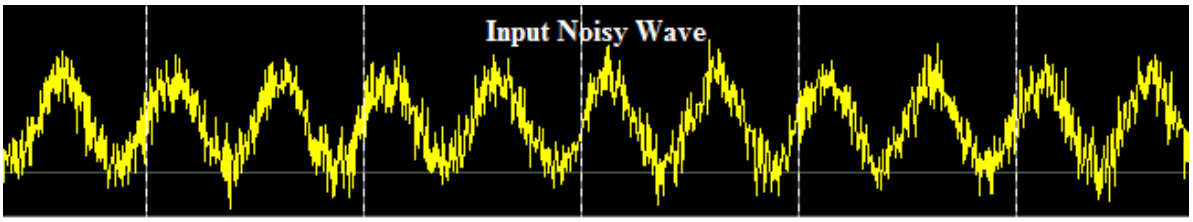


Figure 3.13(a) – showing the input Noisy wave

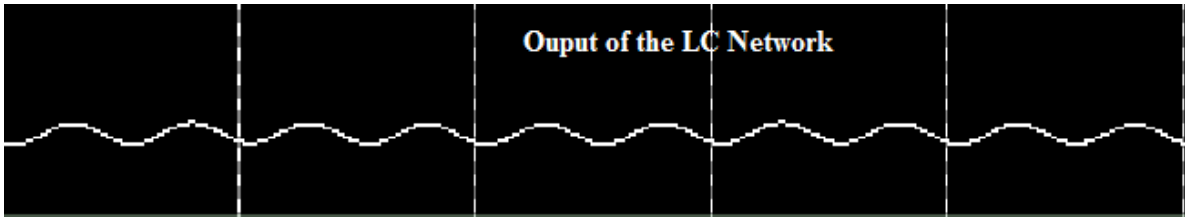


Figure 3.13(b) – Showing the Output of the LC network

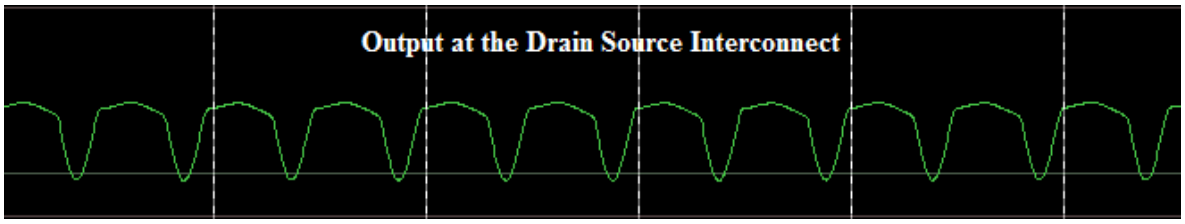


Figure 3.13(c) - showing the output at the Drain-Source interconnect of the MOSFETs

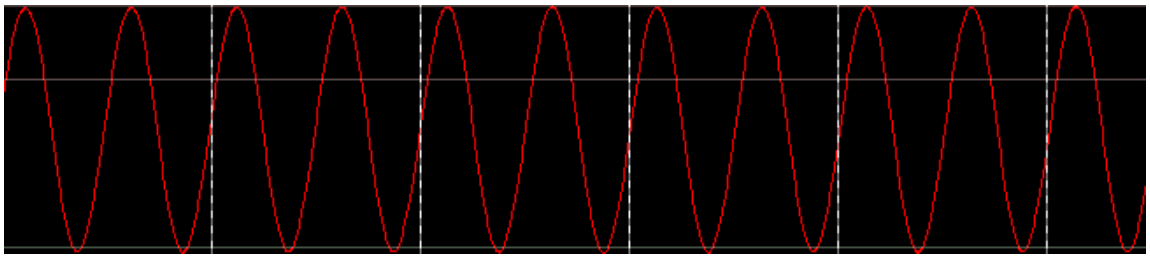


Figure 3.13(d) – showing the Final output of the circuit filtered out of noise.

The above circuit operation outputs show how the noise in the circuit gets filtered at each stage and how we get a noise-free output at the output of the circuit.

The various stage filtering by the various components of the circuit followed by the effect of the huge parasitic capacitance smoothen the wave, reducing the noise components in the output of the circuit. Thus the Noise filtering capabilities of the circuit model were studied in detail.

CHAPTER 4

RESULTS AND INTERPRETATIONS

The various aspects of LNA design were explored and the various factors to be considered while designing a LNA were clearly understood. Various analysis were done on the LNA circuit and also on the various blocks of the circuit like the multi-finger MOSFET design and the spiral inductor model. Based on the simulation results the circuit components were used in the layout to meet the requirements.

The various parameters such as the voltage gain and the input impedance were found out. First we analyze the various parasitic capacitances as extracted the microwind layout tool. The circuit representation of the circuit with the parasitic capacitances is as shown in the figure 4.1.

4.1 Final LNA Circuit :

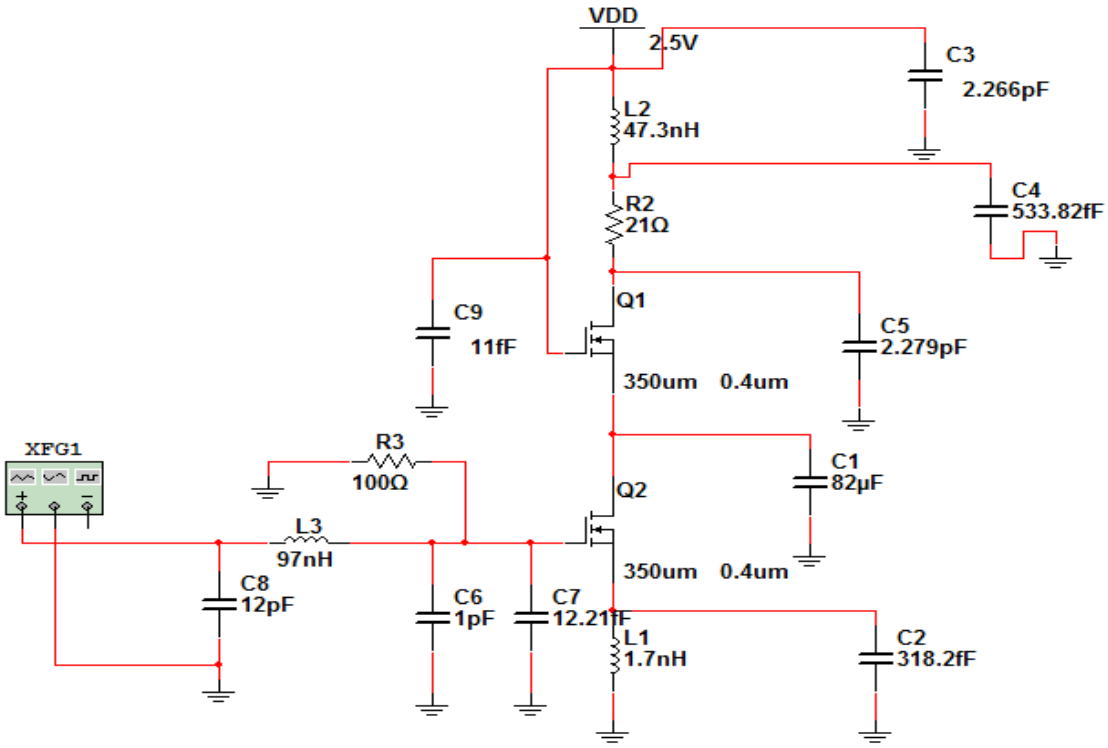
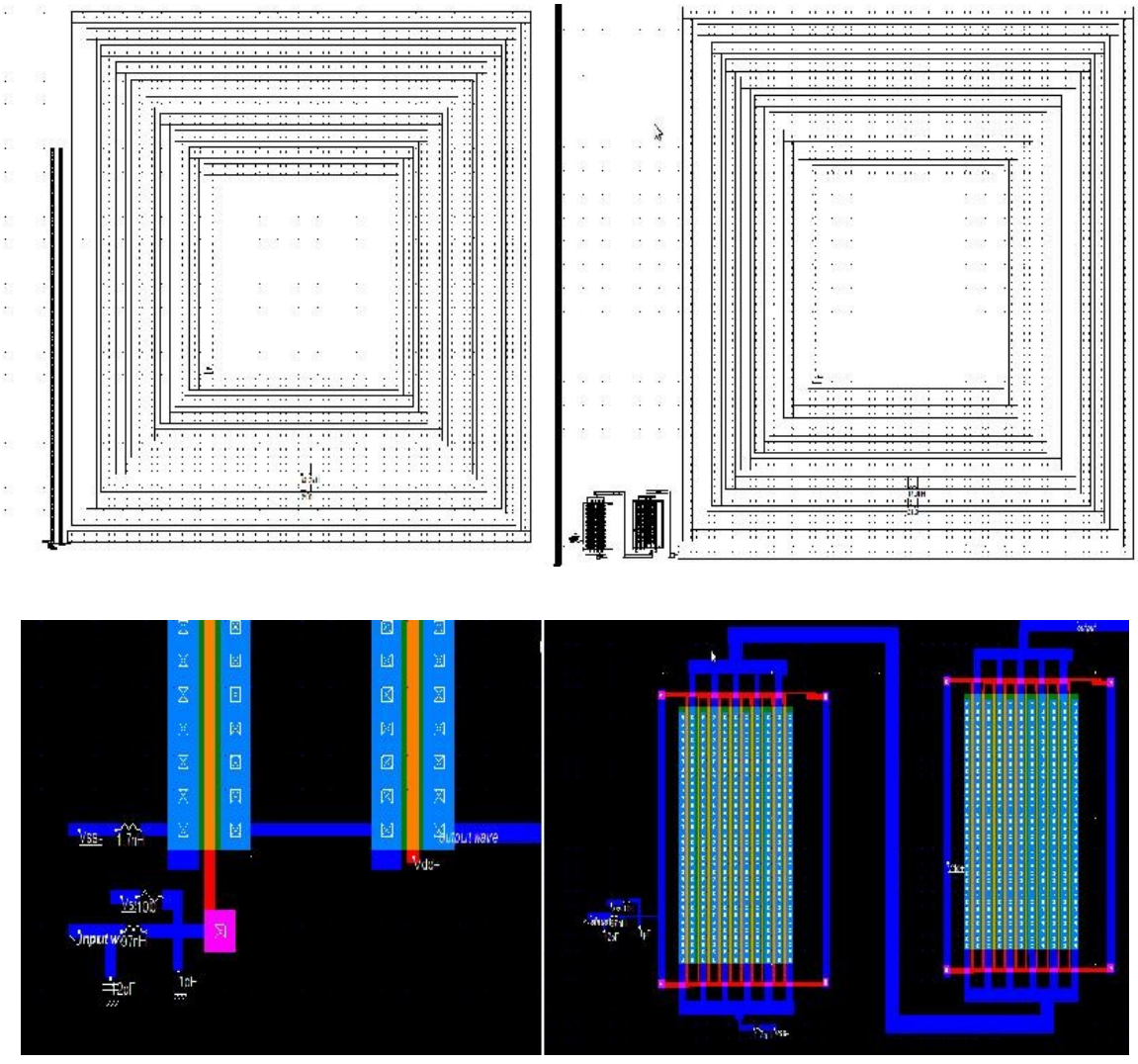


Figure – 4.1 Showing the schematic representation of the final LNA circuit with the parasitics as generated by Microwind

As from the schematic representation the MOSFETs used are of the dimension of 350µm and length of 0.4µm. The spiral inductor model used is a single layered metal (metal 1) inductor with an inductance value of 47.3nH and 21 ohms resistance with a Q-factor value of 2.03. The circuit is properly biased by giving an off-set voltage at the input which is equal to V_{DD} /2 so that the transistors are operated in the liner region. It is also important to note that the Cascode configuration makes it important to give a proper biasing so that both the transistors are functioning properly.

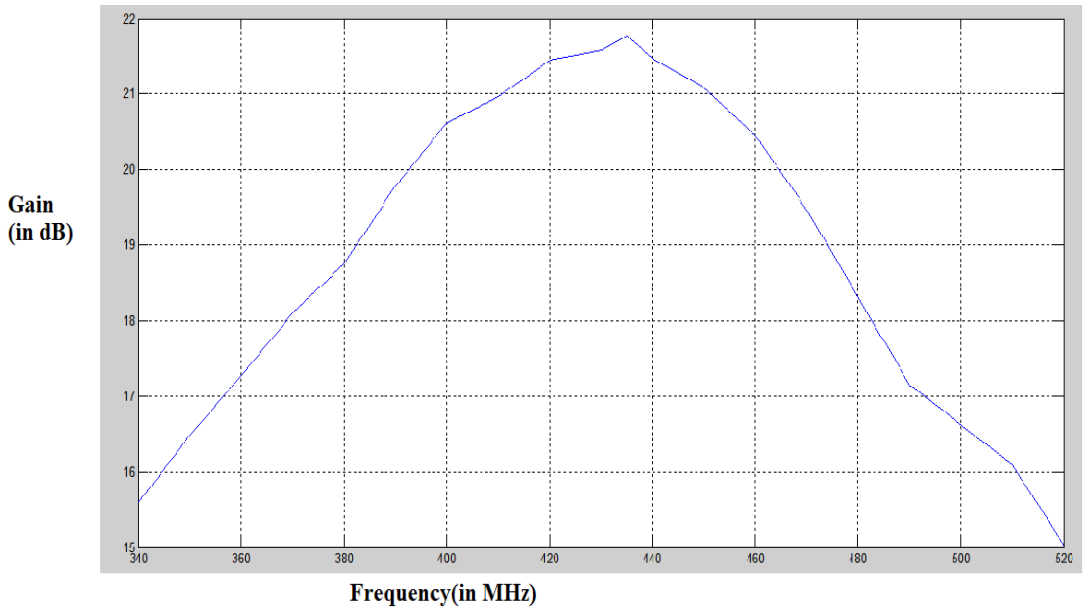
The layout of the circuit implemented is shown in the figure 4.2 below.



The layout to the left correspond to the long MOSFET model and the figures to the right correspond to the multi-finger MOSFET implementation.

4.2 Gain vs Frequency Plot:

The multi-finger MOSFET Design offers a peak gain at 446MHz and the long MOSFET design offers a peak gain at 435MHz which is due to the change in the output capacitance of the circuit. The peak gain of the Long MOSFET model is at 21.766dB and that of the multi-finger MOSFET design is 21.626dB. The circuits differ in their output capacitance which affects the tapering off of the gain values as we move the operating frequency on both sides of the peak frequency. The Gain vs Frequency Plot of the circuit is as given in the Figure 4.3 below.



Upon close examination of the Gain vs Frequency plot shows that the frequency tapers off rapidly on both the sides of the peak gain frequency of 435MHz and this tapering off is desired

4.3 Noise Filtering:

The factors affecting the filtering and the filtering effect of the various circuit components of the circuit were discussed earlier and thus the circuit provides good Noise-free output. This is shown in the figure 4.4.

The good noise filtering is attributed to the good filtering at the input and the parasitic capacitances that smoothen the wave. The filtering is affected by the parasitic capacitances as they are too large to be ignored.

4.4 Input Impedance and Output Impedance:

The input circuit is the same as the input stage circuit in the reference paper[1]. The inductor Ls provides a real part to the input impedance at the gate of M1. That real part which is in the order of 100-150Ω is reduced to lower values due to the presence of the parasitic capacitance impressed by the pad and ESD parasitics. The real part and the imaginary part of the input impedance is then matched to 50Ω through off-chip matching elements. The 50ohm input impedance is a good value considering that it matchs the impedance of an antenna as an LNA usually follows the Antenna.

The equal size transistors M1 and M2 constitute a cascode configuration that lowers the Miller capacitance preventing the input impedance degradation. Cascode configuration also provides increased input-output isolation.

The output impedance of the circuit was measured in Multisim to be a very high value . Thus it acts as a good match for further stages.

The fabrication steps of the circuit as given by the 3-dimensional modeling of the Microwind software is as shown in the figure 4.3

Table 4-1 – showing the various parameters of the final LNA

Parameters	Value
Peak Gain Frequency	435MHz
Bandwidth	100MHz
Peak gain	21.766dB (12.255)
0-dB frequency or Oscillating Frequency	750MHz
g_m(for the transistors)	242milli Siemens
Power Supply V_{DD}	2.5V

The 3-dimensional Fabrication procedures as given by microwind is given in the figure below showing the important steps.

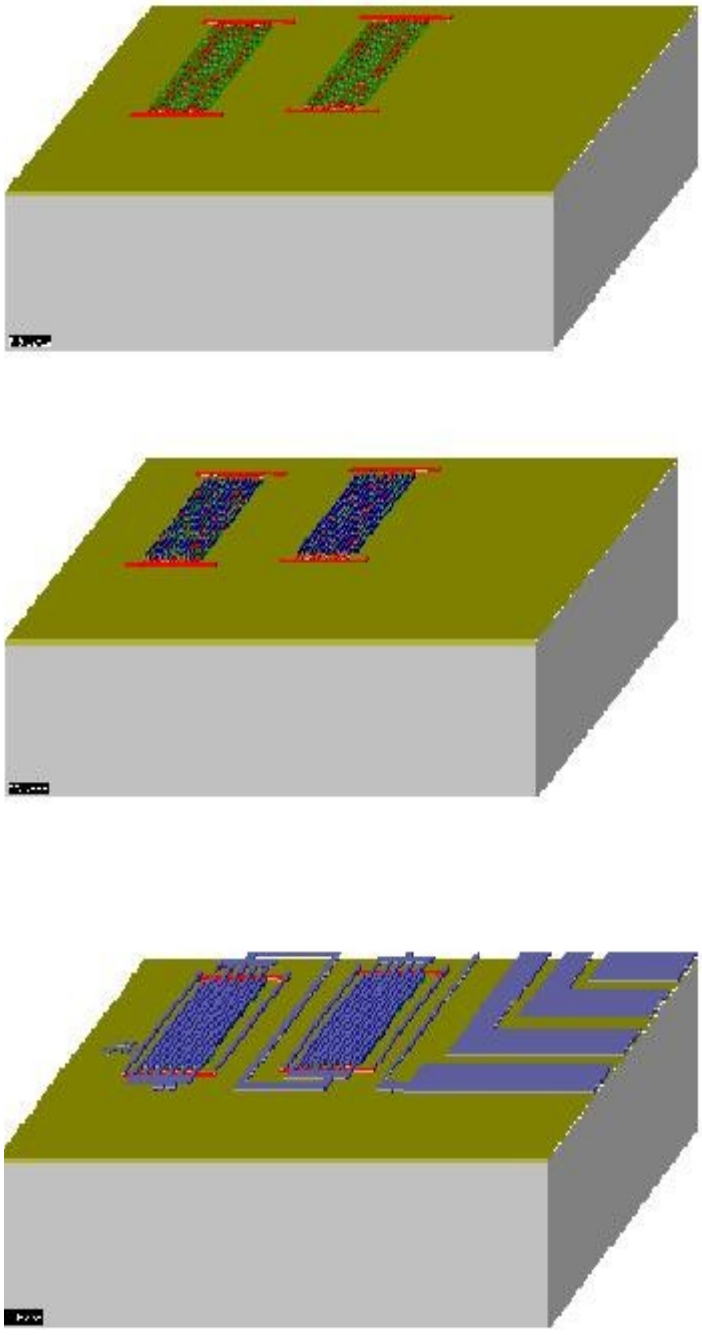


Figure – showing the important steps in the fabrication of the circuit

CHAPTER 5

SUMMARY AND CONCLUSION

By taking into account the specifications for the first-stage LNA, the objectives established at the beginning of the project were largely achieved. The desired frequency range, voltage gain, and input impedance were achieved by selecting the appropriate circuit topology. By using low bias currents, the total current consumed by the LNA was reduced. Meanwhile, by ensuring that the noise due to resistors did not affect the AC operation of the circuit, the noise was minimized.

\ Microwind layout design tool is unique in itself that it generates the parasitic capacitances and simulates the circuit with the effects of these parasitics. This unique feature was used in understanding effects of these parasitics on the circuit components. This circuit level analysis along with the parasitic effects gave me an industry level experience as to how an IC (Integrated circuit) is designed to meet the requirements of the customer and then how it is designed into the layout form to get the final deliverable ,that is, a chip.

The unavailability of the various process technology parameters and stack height has lead to limited freedom in analyzing the circuit and matching the various individual blocks. The various stages of analyzing the components of the circuit were done and from the simulation results the components that best suited the requirements of the LNA were chosen. The Cascode amplifier advantages were studied and also compared it with a single stage amplifier. The advantages of using a Spiral inductor and the parameters that go into the design of these inductors were studied and carefully implemented. The knowledge to analyze and the netlist and come out with inferences was also gained in the process.

Even though the design of the LNA was the primary goal an in-depth understanding regarding the various primary models of inductors, modeling of MOSFETs also achieved. The project which was given to me by IBM through the remote-internship program gave me an experience of the various challenges as faced by the industry and the various stages through which a chip reaches a customer and how it's performance is assured.

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