Generation of Electrical Solitons in 180nm CMOS Technology using Adaptive Bias Controlled Ring Oscillators

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Abstract

The progressive miniaturization seen in the current era of nanoelectronics poses the significant problem of signal distortion. Taking cue from the concept of solitons introduced in recent times in optical and electronic domains, the present work proposed a new perspective on the design of a Solitary Pulse Generator Circuit. The key elements here are Ring Oscillators consisting of CMOS inverters, in whose feedback path a potential divider circuit is inserted. It is seen that the potential divider provides significant altering of Operating Point, thus transforming Ring Oscillators to Adaptive Bias Controlled Ring Oscillators (ABCRO). The output is characterized using waveforms and spectra, and a decent match with conventional hyperbolic secant based solitary pulses is observed. The effect of supply voltage on frequency and power dissipation, and the effect ofnumber of stages are also studied. The simplicity of the proposed design in comparison with conventional soliton oscillators, coupled with low values of power dissipation and consistent frequency of operation form the significant highlights of the present work.

Keywords: Solitary Pulses, Ring Oscillators, MOSFET Nonlinearity, Microwind, 180nm CMOS

1. Introduction

The current era of nanoelectronics has ushered in an unprecedented progress in minitiurization, scaling down circuits and devices to lower and lower technology nodes [1, 2]. However, when such circuitry are used in real-life communications and computing based applications, one encounters the crucial problem of signal distortion [3]. Some factors affecting signal distortion in nanoelectronic circuits include noise and intermodulation [4, 5, 6, 7]. However, the key contributors to signal distortion, especially in logic systems that typically use square wave based clocks, are the wiring parasitics [8, 9]. Since the back-end-of-line (BEOL) interconnects of a typical integrated circuit can be modeled as transmission lines, one observes a low pass filtering effect provided by such wiring interconnects [10, 11, 12, 13]. As a result, the high frequency components of a square wave are significantly attenuated, heavily distorting the waveform shape [3]. One logical solution to this problem would be to replace square wave based clocks with signals whose high frequency components are not much prominent [14, 15].

Recent research and advances in the field of optical communications have provided a fresh perspective to the above mentioned problem through the concept of Soliton [16, 17]. Typically, solitons are viewed as mathematical solutions to nonlinear partial differential equations such as the Nonlinear Schrodinger Equation (NLSE), which describe pulse propagation through an optical fiber considering various dispersive and nonlinear effects [16]. A characteristic feature of the Solitary Pulse is its 'bell shape', typically described as a Gaussian or Hyperbolic Secant Function [14, 15, 16]. Taking cue from these results, successful attempts have been made to generate electrical solitons, where, a transmission line periodically loaded with varactors, acting as a Nonlinear Transmission Line, is coupled with an adaptive bias controlled amplifier, the whole circuit acting as a electrical soliton oscillator [18, 19, 20]. Also, it has been shown that in prototype Terahertz frequency communication systems such as Radio over Fiber involving both electrical and optical channels, soliton based carriers exhibit significantly lower distortion than the square and sinusoidal counterparts [14, 15].

The present work purports to an alternate approach to the generation of solitary pulses. Specifically, a ring oscillator is designed and by proper manipulation of a potential divider circuit in the feedback path ('ring') of the circuit, appropriate waveshaping can be achieved leading to the generation of solitary pulses. By examining the match between the generated output and a hyperbolic secant based solitary pulse, the solitary nature o the output is ascertained. By various parametric analysis studying the effect of supply voltage on the power dissipated and oscillation frequency it is concluded that the proposed design provides a simpler and power efficient alternative to the conventional soliton oscillators, and these form the main highlights of the present work.

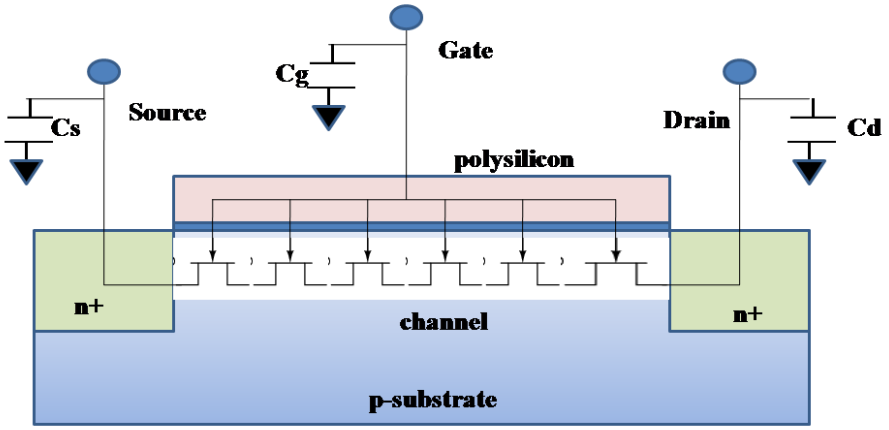

Figure 1: Non-quasi static representation of a NMOS channel

2. Design and Methodology

In this section, various design aspects pertaining to the solitary pulse generator are discussed.

2.1. Nonlinearity in a CMOS Inverter

The primary component of the proposed solitary pulse generator is a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [1]. It is well known that due to the presence of three modes of conduction (cut-off, linear and saturation), the MOSFET is prone to and exhibits nonlinear behavior. This behavior of a single N-Channel Enhancement MOSFET (NMOS) can be described by the following expression [21]:

$$I_d = \frac{\mu_n Z C_i}{L}\left[\left(V_G - V_{FB} - 2\psi_f - \frac{V_D}{2}\right)V_D - \frac{2}{3}\frac{\sqrt{2\epsilon j_s q N_a}}{C_i}\left[(V_D + 2\psi_f)^{1.5} - (2\psi_f)^{1.5}\right]\right] \quad (1)$$

Here μ_n denotes the electron mobility, C_i the intrinsic capacitance, V_{FB} is the flat band voltage, j_s is the current density, q is the charge, N_a is the acceptor concentration, ψ_f denotes the work function, L denotes the channel length and Z denotes the channel width, both of which are the key transistor geometry parameters. Throughout the present work, a technology node of 180nm is chosen, thus resulting in a λ value of 90nm, and all NMOS and PMOS transistors are scaled to an aspect ratio of $2\lambda \times 6\lambda$. The whole implementation is carried out using Microwind, a deep submicron VLSI layout design software using a 180nm CMOS technology [22]. The device parameters and equations employed in the Microwind implementation are obtained from BSIM4 modeling [23].

The fractional exponents in the above equation represent the NMOS nonlinearity. Another significant factor contributing to MOS nonlinearity, particularly at high operating frequencies is the non-quasi static charge model of the MOS channel, which states that the channel of a MOSFET can be modeled as a nonlinear transmission line [24]. An illustration of the NQS model applied to the NMOSFET along with the drain, gate and source capacitances is shown in Fig.(1). Also, the equivalent representation of the nonlinear transmission line is seen as an Elmore resistance, which is length dependent and indicates the effect of wiring and transistor geometry in generation of solitary pulses. The equivalent circuit of Fig.(1), with the Elmore resistance denoted by 'Re' is shown in Fig.(2). The dependance on the Elmore Resistance on the gate-source voltage V_{gs} is given as follows [24]:

$$Re = \frac{L_{eff}}{10\mu_{eff} W_{eff} C_{ox}(V_{gs} - V_{th})} \quad (2)$$

where μ_{eff} is the effective carrier mobility, L_{eff} and W_{eff} denote the effective channel length and width of the NMOS transistor, C_{ox} denotes the oxide layer capacitance and V_{th} is the threshold voltage of the transistor.

As a result of the above mentioned factors, when NMOS and PMOS are connected to form a CMOS inverter, one typically observes nonlinear behavior in the transition regions between the 'HIGH' and 'LOW' states [22]. To understand this better, a transfer curve between the input and output of a single stage CMOS Inverter in 180nm technology is shown in Fig. (3). The obtained transfer characteristics have been fitted with a sigmoid of the following form, where Vx and

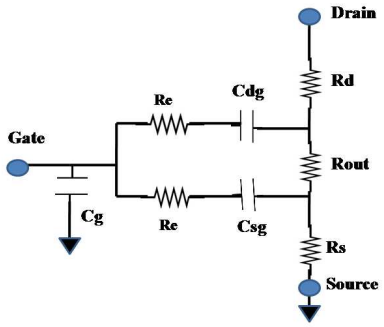

Figure 2: Equivalent circuit of non quasi static channel effect

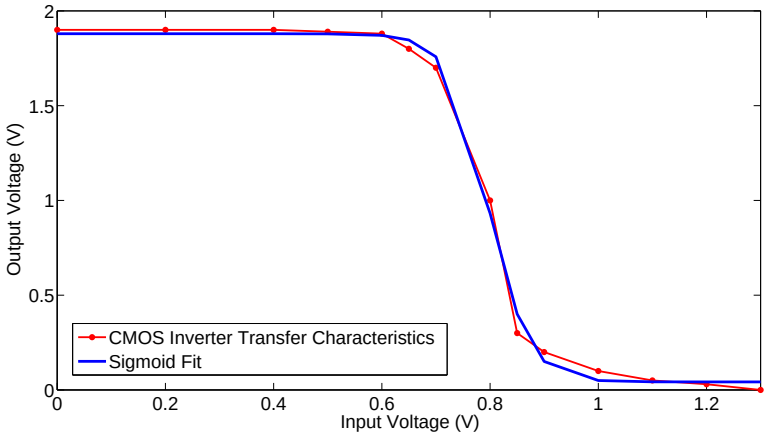

Figure 3: The transfer characteristics of a CMOS Inverter as obtained from Microwind (red), with a sigmoid fit for the same (blue)

Vy represent the Input (Common Gate) and Output side Signals respectively. From the plot, it can be seen that the key nonlinear transition points of the transfer curve lie at around 0.7V and 1V of the input voltage Vx.

$$Vy = 0.0421 + \frac{1.8372}{1 + 10^{-11.7657(0.7977 - Vx)}} \tag{3}$$

2.2. The Ring Oscillator

A Ring Oscillator is a resonator-less Oscillator formed by connecting in a closed loop, an odd number of inverters [25]. Since in odd number of inverters, the output of the last stage is a complement of the input to the first stage, this creates a theoretically endless cycle of instability, witnessed by the continuous alternating between low and high states. The time period of the ring oscillator output is given by the relation [25]

$$T = 2MT_d \tag{4}$$

where M denotes the number of stages and T_d is the delay of each stage. Due to this principle, the Ring Oscillator is used as the oscillating element in the proposed design.

In a given technology, a ring oscillator consisting of 3 stages is the simplest possible ring oscillator design. In order to study the behavior of this configuration, a 3 stage ring oscillator is designed, as shown in the schematic and layout in Fig. (4) and Fig. (5) respectively.

The output waveforms for each stage of the Ring Oscillator (denoted as 'RO') are plotted in Fig. (6). The corresponding FFT spectra are shown in Fig. (7).

From the plots, it can be seen that the higher frequency components (such as at 30-40GHz) are more dominant in stages RO1 and RO2, and decreases in the output RO3. As a result, the harmonics visible in the pulse waveform of RO2 are filtered out in RO3 and produce a more sinusoidal-like output.

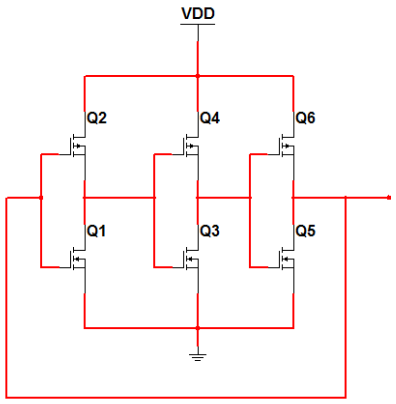

Figure 4: The Schematic of a 3 stage Ring Oscillator

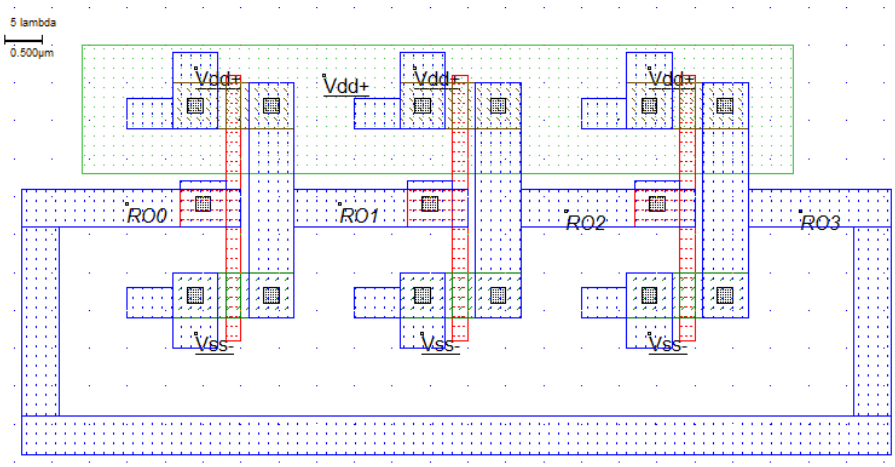

Figure 5: The Layout of a 3 stage Ring Oscillator

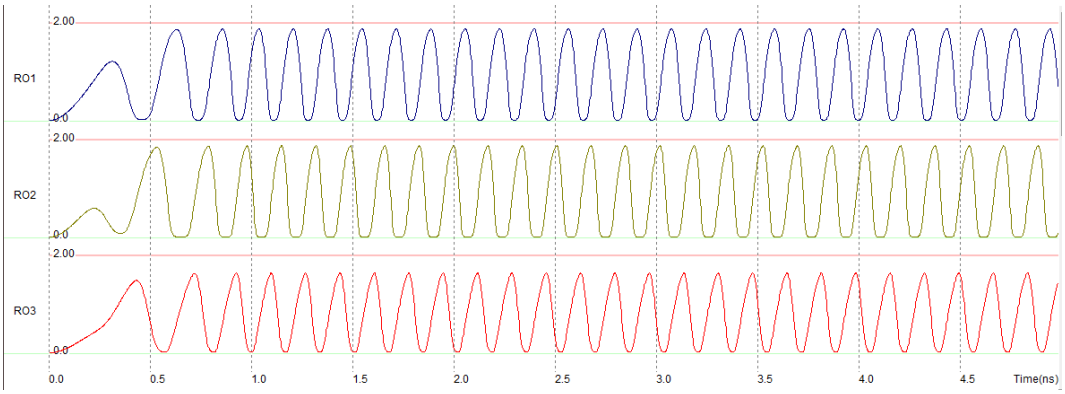

Figure 6: The output waveforms of the 3 Stage Ring Oscillator. The stages are denoted by RO0, RO1, RO2 and RO3. In this case, RO0 and RO3 refer to the same node.

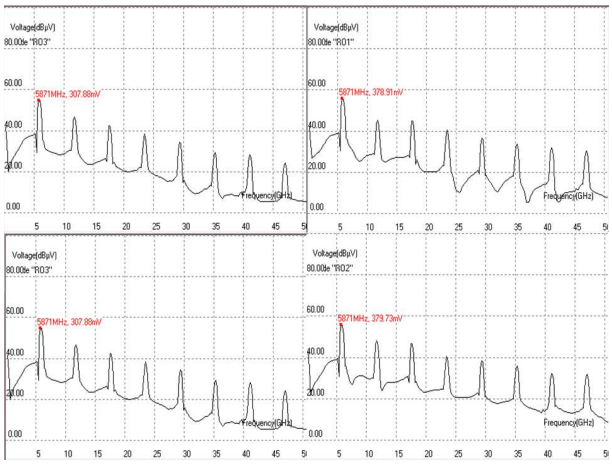

Figure 7: The output FFT Spectra of the 3 Stage Ring Oscillator. The stages are (clockwise from top left) RO0, RO1, RO2 and RO3. In this case, RO0 and RO3 refer to the same node.

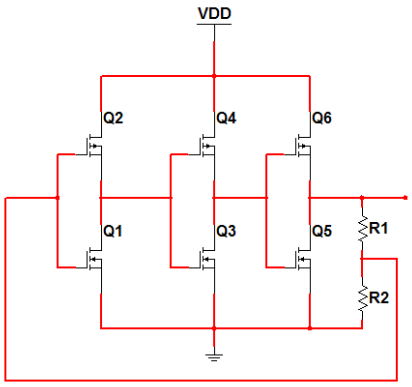

Figure 8: The Schematic of a 3 stage Ring Oscillator with Adaptive Bias Control

However, there are two significant problems in the Ring Oscillator circuit. Firstly, the loading conditions have not been considered, and secondly, the output waveforms exhibit features of sinusoid and lack crucial harmonics seen typically in a solitary pulse [16].

2.3. The Solitary Pulse Generator

Taking cue from the above mentioned results, the present work proposes a design where the coupling between the third stage output and first stage input of a ring oscillator is given through a resistive potential divider. The schematic and layout are shown in Fig. (8) and (9).

By setting the value of R1 and R2 to 20kΩ and 100kΩ respectively, the potential dividing factor is set to a value of 0.2. It should be noted at this juncture that the use of a potential divider in the 'ring' enables significant manipulation in the amplitude of oscillation given to the first stage input. This consequently affects the operating point of the first inverter, according to the characteristics shown in Fig. (3). It is for this reason that the proposed design is termed the 'Adaptive Bias Controlled Ring Oscillator', or ABCRO. The voltage waveforms and FFT Spectra at each stage of the ABCRO are plotted in Fig. (10) and Fig. (11).

From the plots, it is observed firstly that ABCRO0 and ABCRO3 are separate nodes, unlike RO0 and RO3 in the case without adaptive bias, and that the potential divider and the interaction with its resistors with the wiring parasitics enable significant waveshaping and attenuation of the ABCRO3 output. Furthermore, the resistors in the potential divider also act as loads for the circuit. From the spectra, one observes that the amplitudes of higher frequency components (such as 20-40GHz) show significant increase as one progresses from ABCRO0 to ABCRO3. However, all this is achieved at the expense of a decrease in the fundamental frequency component (repetition rate of the solitary pulses) from 5.87GHz in RO to 3.974GHz in ABCRO.

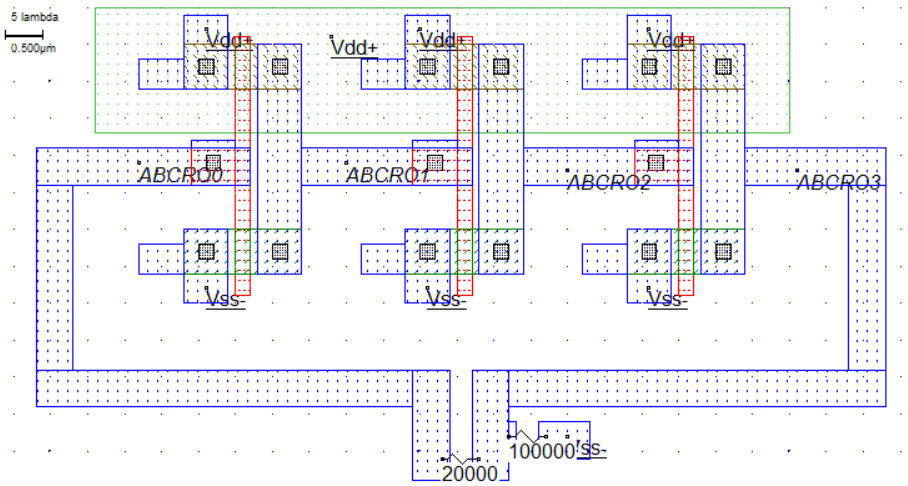

Figure 9: The Layout of a 3 stage Ring Oscillator with Adaptive Bias Control

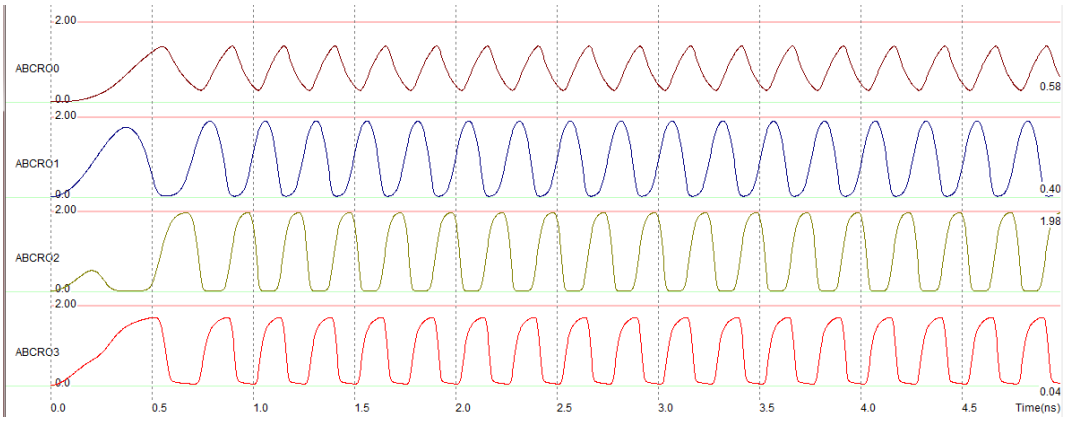

Figure 10: The output waveforms of the 3 Stage Ring Oscillator. The stages are denoted by ABCRO0, ABCRO1, ABCRO2 and ABCRO3.

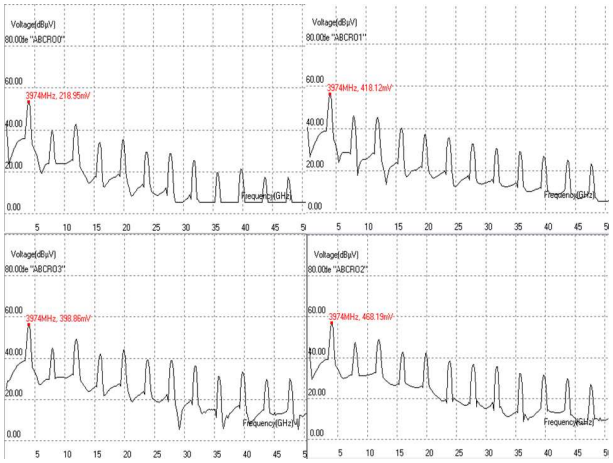

Figure 11: The output FFT Spectra of the 3 Stage Ring Oscillator. The stages are denoted by ABCRO0, ABCRO1, ABCRO2 and ABCRO3.

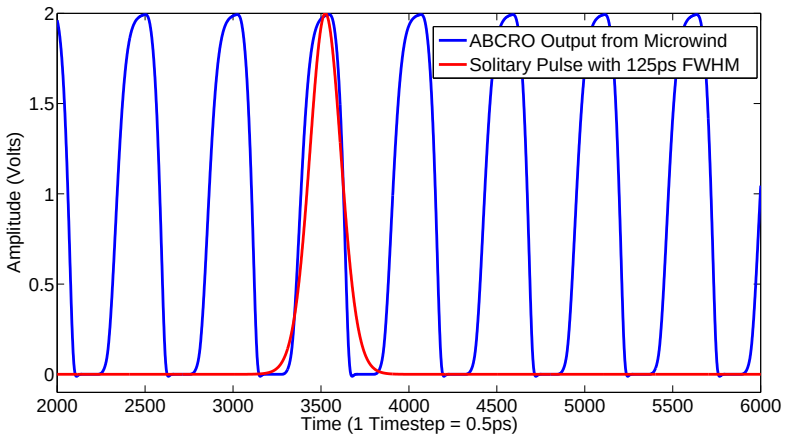

Figure 12: Obtained pulse train at ABCRO3, with a single pulse fitted to a hyperbolic secant based solitary pulse ($sech^2$) with a Full-Width Half Maximum (FWHM) at 125ps.

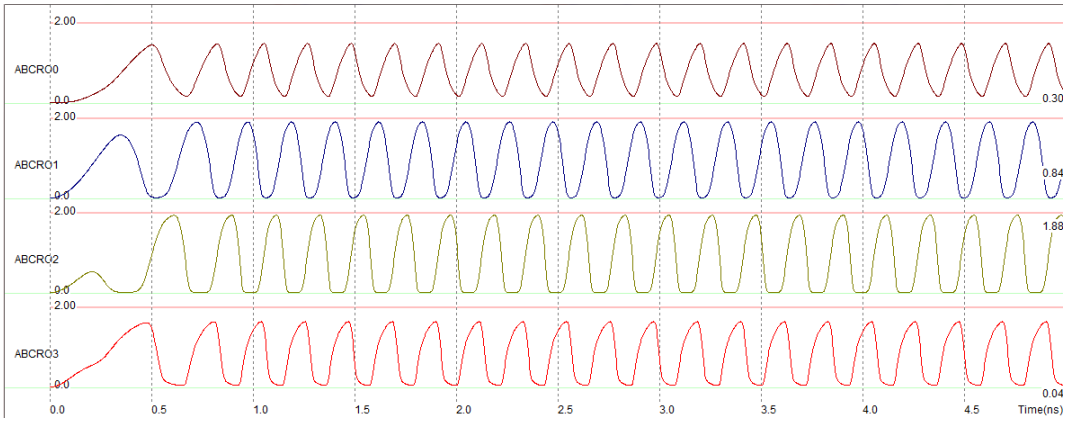

Figure 13: Output waveforms at each stage of ABCRO with potential divider ratio set to 0.1

3. Results and Discussion

3.1. Solitary nature of obtained pulses

From Fig. (10) and Fig. (11), it is evident that the addition of a potential divider in the ring oscillator circuitry provides the necessary operating point shift and hence waveshaping in order to generate pulses. In order to ascertain the solitary nature of the obtained pulses, a single pulse among the pulse train of ABCRO3 in Fig. (10) is fitted to a hyperbolic secant ($sech^2$) based pulse and is shown in Fig. (12) [16]. It is seen that the pulses generated from the ABCRO reasonably approximate the hyperbolic secant based solitary pulses, with the proposed design becoming one of the simplest ways to generate such pulses.

3.2. Effect of Potential Divider Ratio

Since the potential divider affects the operating point of the first inverter, it is a key component of the waveshaping and hence pulse generation. In the implementations discussed in the above section, the potential divider ratio was set to 0.2. However, to study the effect of the potential divider ratio, the resistor R1 is changed to different values such as 10 kΩ, 50 kΩ, 100 kΩ and 200 kΩ, thus altering the ratio between 0.1 and 2, and the corresponding output waveforms are plotted in Fig . (13) - Fig. (16) respectively.

From these plots, it can be seen that as the potential divider ratio is increased from 0.1 to 2, the amplitude of the input ABCRO0 decreases, as a result of which the output of ABCRO3 becomes flatter, approximating a square wave, significantly increasing harmonic content. Additionally, the fundamental frequency decreases. Thus, among all the potential divider values discussed, it can be seen that 0.2 provides an optimal value, with the generated pulse most closely resembling a solitary pulse, as shown in Fig. (12).

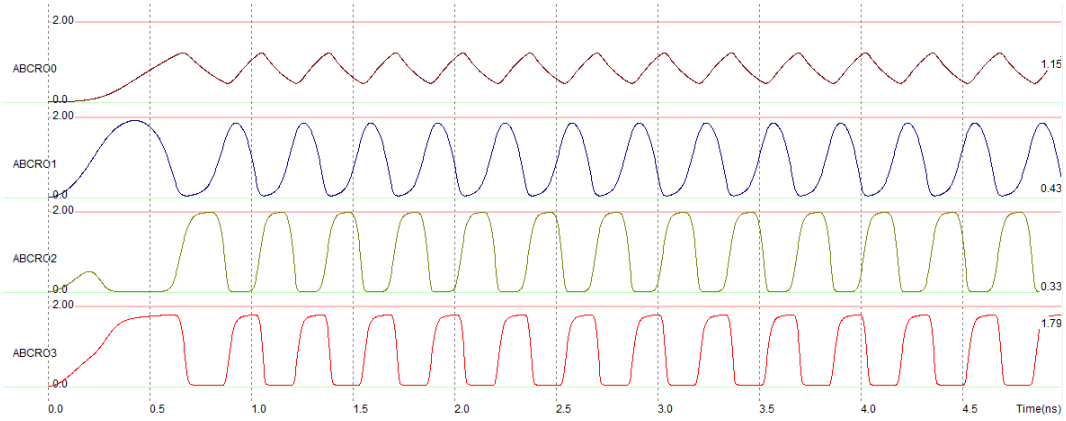

Figure 14: Output waveforms at each stage of ABCRO with potential divider ratio set to 0.5

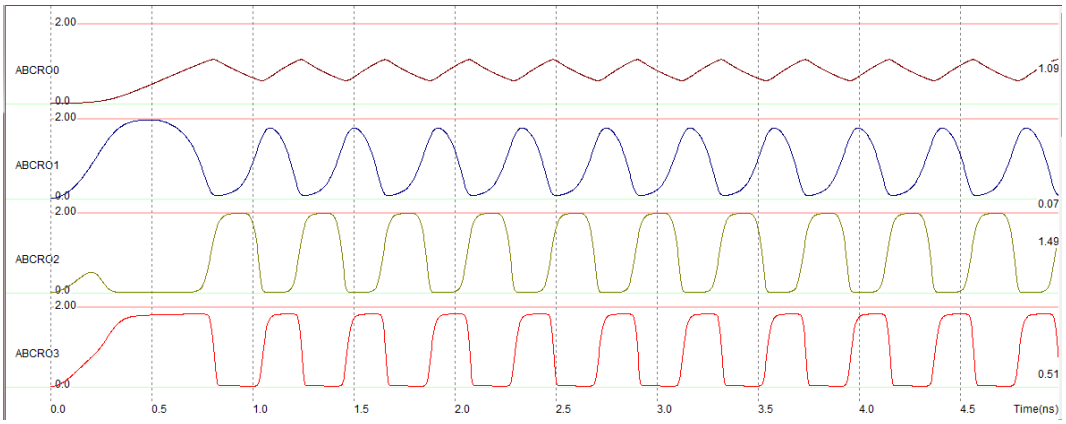

Figure 15: Output waveforms at each stage of ABCRO with potential divider ratio set to 1

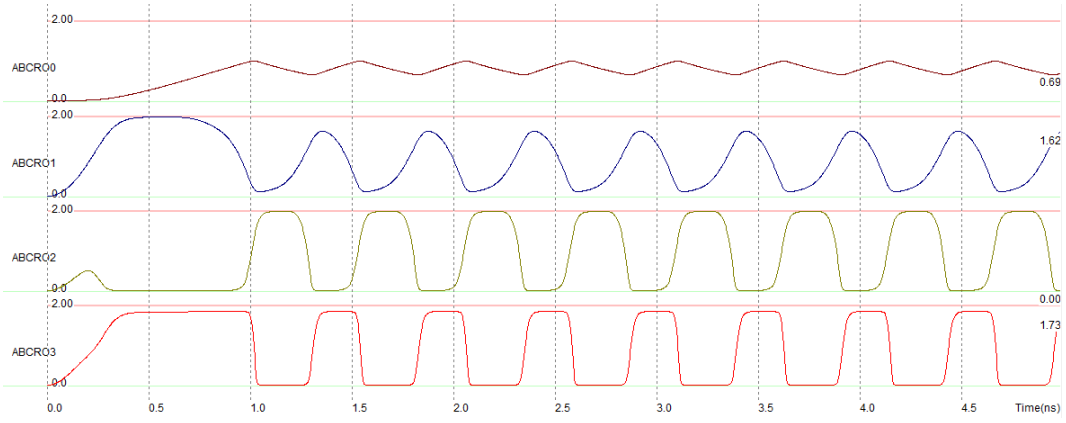

Figure 16: Output waveforms at each stage of ABCRO with potential divider ratio set to 2

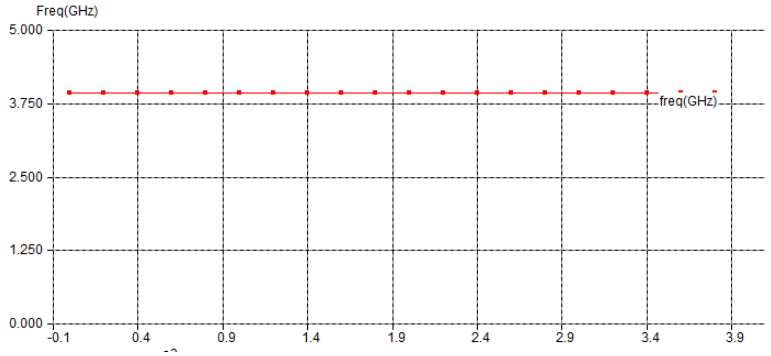

Figure 17: Variation of fundamental frequency of ABCRO3 as a function of Supply Voltage

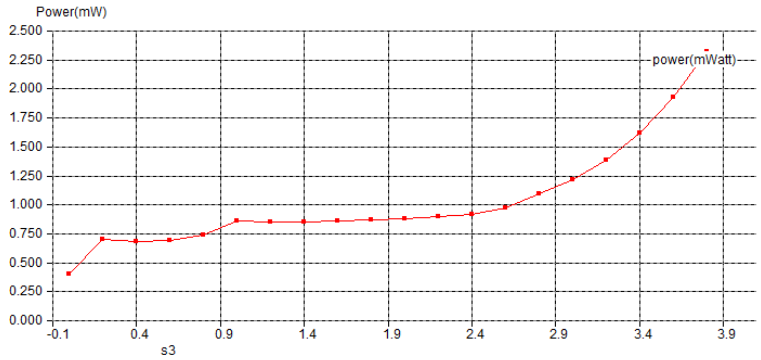

Figure 18: Variation of power dissipated of ABCRO3 as a function of Supply Voltage

3.3. Parametric Analyses

Keeping the number of stages fixed at three, and keeping the potential divider ratio fixed at 0.2, the key significant variable in the ABCRO now becomes the supply voltage V_{DD}. In order to study the effect of the supply voltage on the generated frequency, a parametric analysis is performed, varying the supply voltage from 0V to 4V in steps of 0.2, and recording the fundamental frequency of ABCRO3 in each case [22]. This is plotted in Fig. (17). It can be seen that irrespective of the supply voltage, the output frequency stays fairly constant at around 3.9GHz.

Additionally, to characterize the power dissipation of the ABCRO circuit, it is necessary to perform a parametric analysis varying supply voltage from 0V to 4V as in the earlier case, but recording the power dissipated [22]. This is plotted in Fig. (18). From the figure, one observes that above a supply voltage of 2.4V, the power dissipated rises exponentially whereas, the slight rise at 0.9V represents the threshold related properties and the nonlinear 'knee' point as observed in Fig. (3).

3.4. Solitary Pulse Generating ABCRO using 5 Stages

Finally, to characterize and study the effect of number of ring oscillator stages on the generation of solitary pulses, a 5 stage ABCRO is explored. The layout is given in Fig. (19).

The output waveforms obtained for three potential dividing ratios, namely 0.1, 0.2 and 1 are plotted in Fig. Fig . (20) - Fig. (22) respectively.

From the plots, it is seen that for similar potential dividing ratios, while the input ABCRO0 shows similar amplitudes for 3 and 5 stage cases, the fundamental frequency has decreased significantly, due to the larger net Time Delay, and the edges are much flatter in a 5 stage ABCRO output than the corresponding 3 stage outputs. This implies that the optimal case achieved for a 0.2 ratio in 3 stage ABCRO would now be achieved for a 0.1 ratio in a 5 stage ABCRO.

4. Conclusion

After briefly reviewing the nonlinear behavior of a NMOS transistor and examining a typical 3 stage Ring Oscillator in 180nm CMOS technology, the paper proposes a novel design to generate solitary pulses consisting of introducing a potential divider based adaptive bias control in the feedback path of the ring oscillator (ABCRO). The ABCRO outputs are studied using Voltage waveforms and FFT spectra, and the waveshaping properties become evident. The

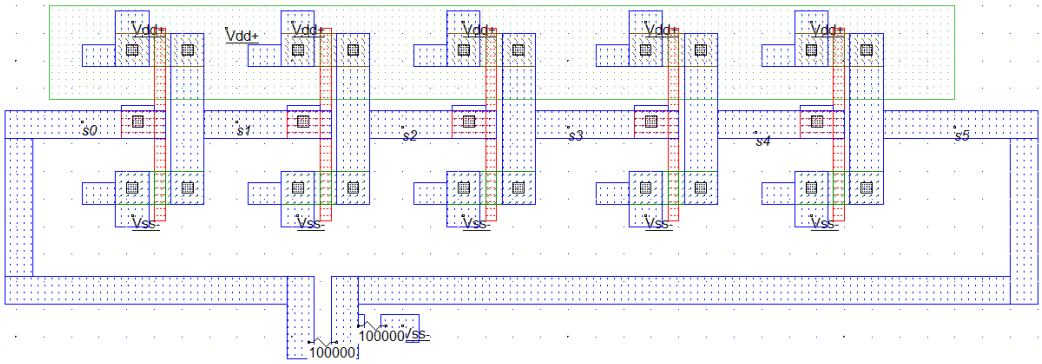

Figure 19: The Layout of a 5 stage Ring Oscillator with Adaptive Bias Control

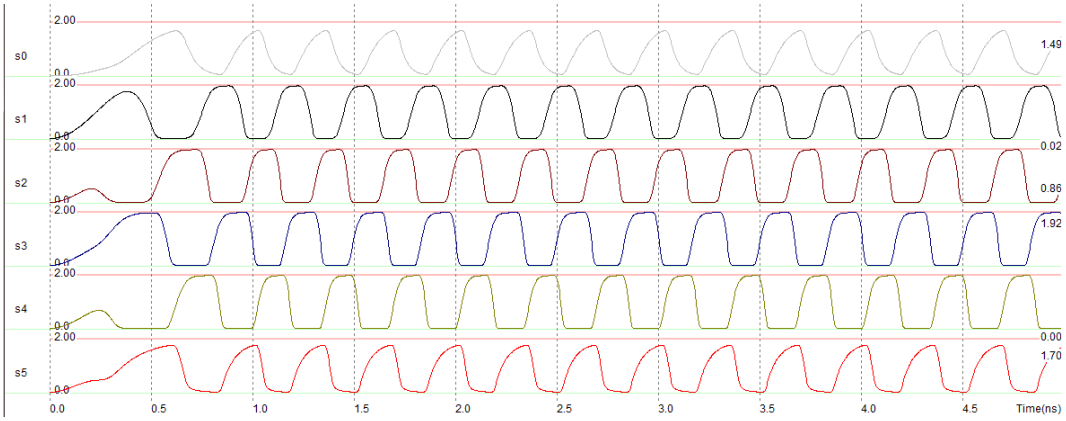

Figure 20: Output waveforms at each stage of 5 stage ABCRO with potential divider ratio set to 0.1

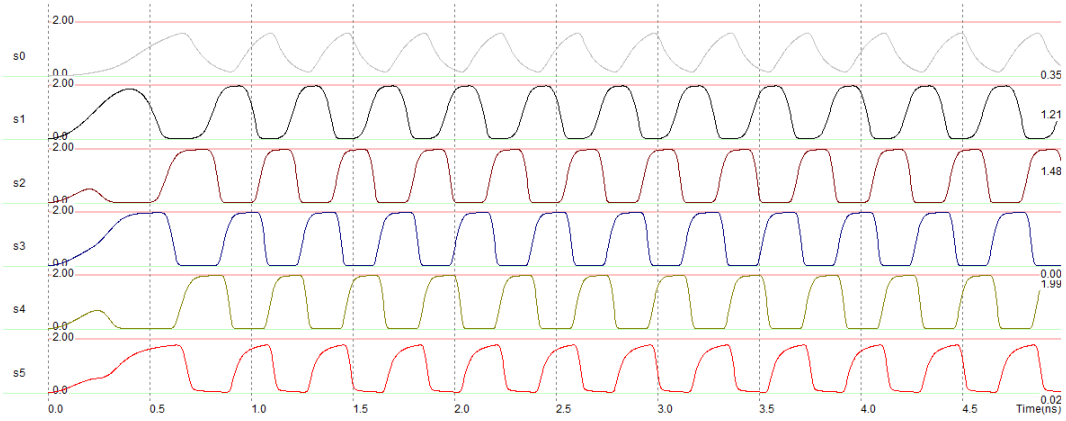

Figure 21: Output waveforms at each stage of 5 stage ABCRO with potential divider ratio set to 0.2

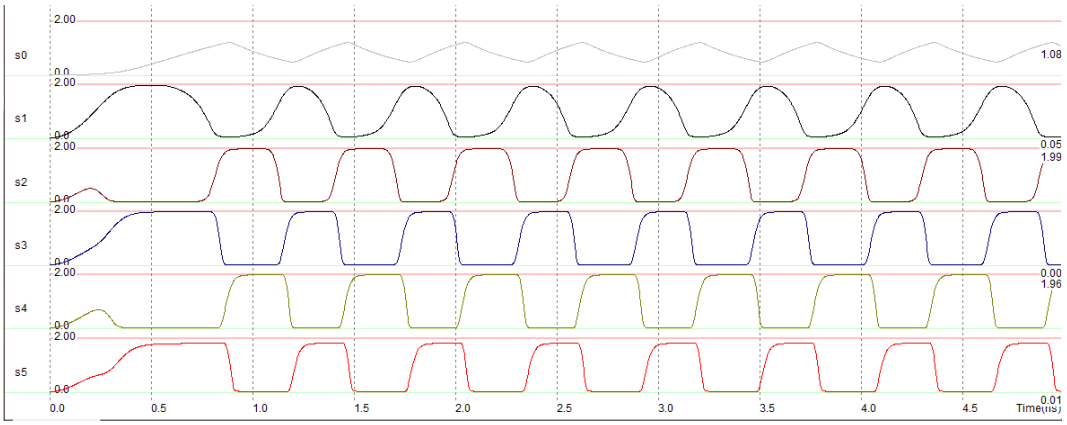

Figure 22: Output waveforms at each stage of 5 stage ABCRO with potential divider ratio set to 1

obtained pulses show a decent match to hyperbolic secant based solitary pulses. The effect of supply voltage on frequency and power dissipated re studied using parametric analyses. Finally, a 5 stage ABCRO is explored. The simplicity of the proposed design in comparison with traditional electrical soliton oscillators, coupled with the low values of power dissipation and consistent frequency observed form the significant highlights of the present work. Further work in this direction would include examining the influence of technology node and type (such as Silicon on Insulator (SOI)) as well as loading and noise effects on the ABCRO output. Also, the adaptive bias part could be changed from the potential divider to various RLC combinations and the outputs observed. The proposed solitary pulse generator finds extensive applications in future generation communications and computing systems where soliton based logic and carriers are used.

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