Harmonic Elimination using Giant-K Planar Filters

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Abstract:

In this paper design of low loss passive planar low pass filter for reducing harmonics in a frequently used voltage source type nonlinear load in low voltage distribution system is proposed. The filter is comprised of a lumped high impedance line inductor made of fused silica and an interdigitated capacitor that is made of $La_{0.5}Na_{0.5}Cu_3Ti_4O_{12}$ giant K material. An extensive simulation of single phase diode bridge rectifier with designed filter is carried out by employing Spice software. The subsequent analyses reveal very low insertion loss for the proposed filter. Furthermore, low total harmonic distortion values conforming to IEEE standards and 3dB cut-off in the range of 75Hz, are obtained. This enables the designed low pass filter to effectively eliminate higher order harmonics over the entire wide band in single stretch. The usage of fractal based capacitor structure with giant K resulting in large capacitance value of the order of 3mF, small size, and the effective harnessing of temperature dependent resistance in the inductor leading to stable cut-off frequency even amidst dynamic load variation form the crux of the present work.

Keywords: Power quality, Harmonic distortion, Planar Filters, Ceramic capacitors

1. Introduction

A power distribution system is said to encompass different types of linear and nonlinear loads. As the linear load draws current in a sinusoidal manner, it does not contribute to generation of power quality problems [1]. On the other hand, in the case of a nonlinear load, non-sinusoidal current with new frequency component is being generated which is instrumental in giving rise to different types of power quality problems. Based on their application, the nonlinear loads can be further classified as domestic and industrial loads. Majority of the domestic loads are single phase in nature. Among the available single phase nonlinear loads, voltage source type nonlinear loads demand special attention owing to their versatile applications ranging from low end applications such as battery charger to high end application such as adjustable speed drives [2], [3]. The present paper pertains to the power quality analysis of domestic nonlinear power loads as shown in Fig. 1.
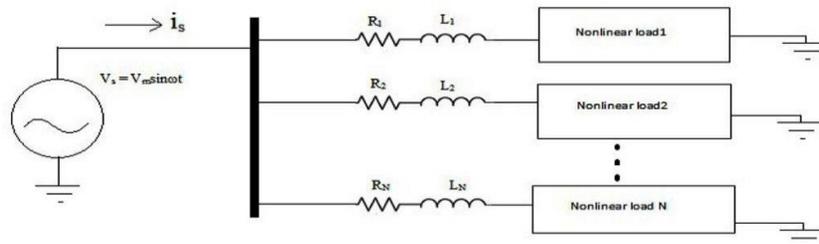

Figure 1 Distribution Systems

According to IEC specifications, in a power system, the power quality is marred by various electromagnetic disturbances such as low and high frequency phenomena pertaining to conduction and radiation, electrostatic discharge and nuclear electromagnetic pulse[4]. Among the various detrimental factors that disrupt the power quality of a given distribution system, harmonics play a crucial role. Furthermore, the proliferation of various single phase domestic nonlinear loads that pertain to the class of unidentified harmonic producing loads in the distribution system are solely responsible for the sporadic increase in the voltage and current harmonic levels in the given system. The harmonic levels, so generated, are highly detrimental to the efficiency of electromechanical energy conversion devices such as motors and transformers. Two main adversaries of the above mentioned harmonic levels are excess heating and loading in electromechanical energy conversion devices.

The present paper portrays a smart passive filtering technique by designing lumped models that constitute an interdigitated capacitor and a planar high impedance line inductor, there by effectively reducing the size of the conventional filter and also improvising its performance. The proposed interdigitated capacitor is characterized by a giant K dielectric material $La_{0.5}Na_{0.5}Cu_3Ti_4O_{12}$ such that comparatively high capacitance value of the order of millifarad's can be obtained. The effective area of the proposed capacitor is designed to be of the order of 20cm 30cm with dielectric thickness of 10mm. The proposed capacitor is specially designed as a fractal capacitor resulting in to wide stop band in the designed low pass filter. On the other hand, a flat strip metal inductor is characterized by a time varying temperature dependant resistance owing to self-heating effects. As a result, the cut-off frequency can be altered to exactly match the harmonic elimination design. Thus a lumped smart single low pass filter with very low cut-off frequency can be designed in such a way that all higher order harmonics can be eliminated at a single stretch, there by resulting in a very low THD value.

2. Design and Methodology

The present work focuses on a single phase diode bridge rectifier considered for the simulation as a nonlinear load. The diode rectifiers used in today's power electronics converters are of this type called voltage stiff type. The assumptions made before simulation are input voltage is sinusoidal and passive components are linear. The source inductance and resistance are assumed as 0.1mH and 0.25 ohm respectively. Supply voltage is 230V; 50Hz.

The proposed filter is a first order low pass filter comprising of lumped inductor and capacitor designed as a planar structure. The lumped inductor in the proposed filter is a fused silica based strip line characterized by its optimal temperature coefficient of resistance which contributes to the harmonic elimination due to self-heating effects.

In order to eliminate the harmonics starting from 100Hz using passive filters, a very high value of capacitance (in mF) is required. This is provided by a lumped capacitor in the proposed filter by resorting to substrate materials that have extremely large relative permittivity (giant K). $La_{0.5}Na_{0.5}Cu_3Ti_4O_{12}$ being a giant K dielectric material having dielectric constant ε_r in the order of 10^5 is found to be an ideal contender for the choice of the substrate [12]-[14]. The geometrical design aspects of the proposed planar filter comprising of the above mentioned lumped inductor and capacitor is given below.

 A. Design of Planar Inductor

The proposed inductor design involves a high impedance line structure comprising of a silica strip whose inductance is given as [15]-[17].

$$L = 0.2 \left\{ ln\left(\frac{l_1}{w+t}\right) + 1.193 + \frac{0.2235(w+t)}{l_1} \right\} \qquad (1)$$

where 'w', 't' and 'l_1' represent the width of the strip (5mm), metal thickness (1cm) and length (1m) respectively of the fused silica strip. The above mentioned structure is illustrated in Fig. 3. Fused silica is chosen as the strip material owing to its ideal temperature coefficient of resistance (TCR) value of 8e-5 K-1. This creates a time varying temperature dependent resistance given by the following thermo resistance equation [18], [19].

$$R(T) = R_0(1 + \alpha T + \cdots) \qquad (2)$$

where 'R' is the equivalent resistance of the high impedance inductor with an initial value of R_0. Using the electro thermal theory for passive devices the time varying temperature is given by [18]

$$T = Ae^{-kx}\cos(\omega t - kx) \qquad (3)$$

where $k = \sqrt{(\omega/2D)}$ and D is the thermal diffusivity.

Substitution of (3) into (2) yields a time varying resistance $R(T)$ which effectively negates the dynamic impedance changes in the nonlinear load such as the diode resistance.

B. Design of Interdigitated Capacitor

Basic capacitance relation is given by $C = \varepsilon_o \varepsilon_r A / h$, where A, h, ε_o and ε_r denote the area of the plate (lw), dielectric thickness, permittivity of free space (2.25×10^{-13} farads/in) and the giant dielectric constant respectively of $La_{0.5}Na_{0.5}Cu_3Ti_4O_{12}$. Finger topology design is primarily used for increasing the interaction area A of the proposed capacitor [14], [16]. The design structure is shown in Fig. 2.

The effect of finger topology on the capacitance is given by the following equation [15]-[17].

$$C = \frac{1 + \varepsilon_r}{w} l \left[A_1(N-3) + A_2\right] \qquad (4)$$

where,

$$A_1 = \left[0.3349057 - 0.15287116\frac{t}{X}\right]^2 ; \; A_2 = \left[0.50133101 - 0.22820444\frac{t}{X}\right]^2 \qquad (5)$$

Figure 3 portrays the finger topology of the proposed capacitor having the following values: l=20cm, w=30cm, N=120 and t=1cm, where l, w, N and t denote the length, width, number of fingers and thickness respectively of the interdigitated capacitor. On substituting the above mentioned numerical values into (4) the capacitance value is obtained to be 3mF. This comparatively large capacitance value is mainly due to the geometrical and material effects of the same.

The significant benefit of using the interdigitated capacitor is that it results in a fractal structure enabling an ultra-wide stop band. To verify the fractal structure of the proposed interdigitated capacitor,

Minkowski Bouligand fractal dimension is calculated [20], [21] using the box counting algorithm with the fractal dimension of the designed structure obtained as 1.52.
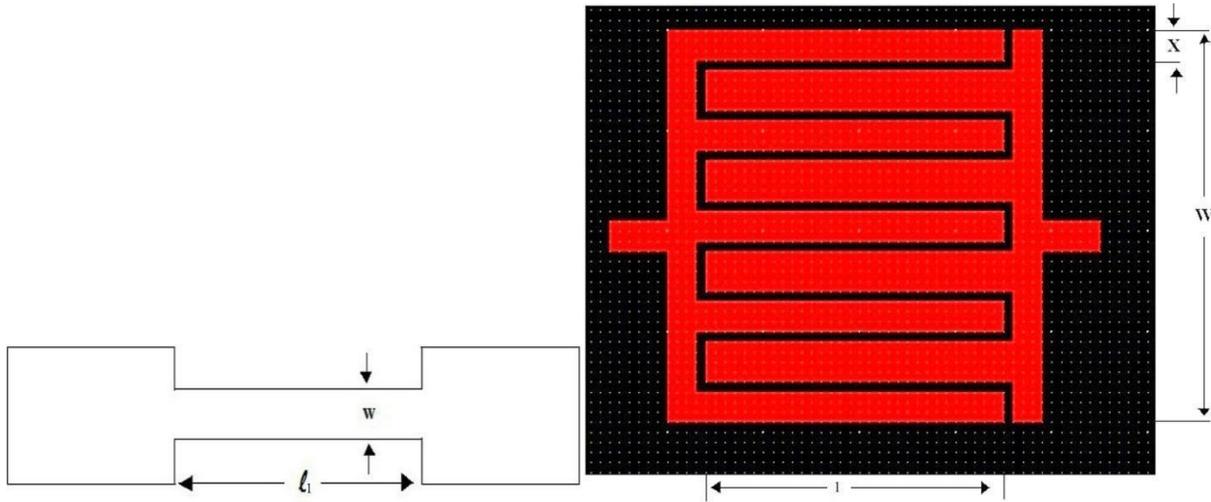

Figure 2 Structure of Inductor (left) and Capacitor (right)

3. Results and Discussion

A. Simulation Results without Filter

The qualitative analysis of the single phase bridge rectifier circuit feeding RC load is performed using the Multisim software. The ensuing simulation results of the same are analyzed in detail at first without the proposed filter by independently changing one of the following parameters namely (i) the load capacitance C_{load} and (ii) the load resistance R_{load}. As is well known, due to the nonlinearity of the bridge rectifier circuit with RC load, the input current gets deformed in to a pulse [1], [4]. Fig. 3 portrays the input voltage and current waveforms, Fourier spectrum and the Fourier analysis for R_{load} =10 ohm and C_{load} = 220 µF.

THD = 52.9119%, Number of Harmonics =20, DC component = 6.87102e^{-005}

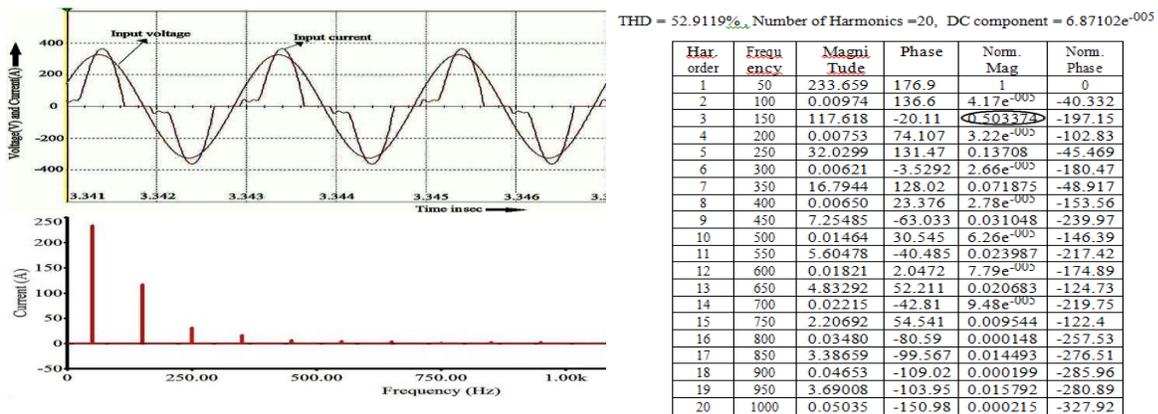| Har. order	Frequency	Magni Tude	Phase	Norm. Mag	Norm. Phase
1	50	233.659	176.9	1	0
2	100	0.00974	136.6	4.17e^{-005}	-40.332
3	150	117.618	-20.11	0.503374	-197.15
4	200	0.00753	74.107	3.22e^{-005}	-102.83
5	250	32.0299	131.47	0.13708	-45.469
6	300	0.00621	-3.5292	2.66e^{-005}	-180.47
7	350	16.7944	128.02	0.071875	-48.917
8	400	0.00650	23.376	2.78e^{-005}	-153.56
9	450	7.25485	-63.033	0.031048	-239.97
10	500	0.01464	30.545	6.26e^{-005}	-146.39
11	550	5.60478	-40.485	0.023987	-217.42
12	600	0.01821	2.0472	7.79e^{-005}	-174.89
13	650	4.83292	52.211	0.020683	-124.73
14	700	0.02215	-42.81	9.48e^{-005}	-219.75
15	750	2.20692	54.541	0.009544	-122.4
16	800	0.03480	-80.59	0.000148	-257.53
17	850	3.38659	-99.567	0.014493	-276.51
18	900	0.04653	-109.02	0.000199	-285.96
19	950	3.69008	-103.95	0.015792	-280.89
20	1000	0.05035	-150.98	0.000215	-327.92

Figure 3 Waveform, Spectrum and THD analysis of diode bridge rectifier without filter

B. Simulation Results with Designed Filter

On substituting $w=5mm$, $t=1cm$ and $l=1m$ into (1) one obtains the value of inductance for a lumped inductor of the proposed filter to be $L=800nH$. The temperature dependent resistance of the silica strip given by (2) is also included while running the simulation.

Owing to its enormous value of dielectric constant ε_r which is approximately of the order of 10^5, $La_{0.5}Na_{0.5}Cu_3Ti_4O_{12}$ material designed as an interdigitated capacitor (as depicted in Fig. 2) acquires comparatively large value of capacitance as is evident from (4). Substitution of $\varepsilon_r=10^5$, $l=20cm$, $w=30cm$, $N=120$ and $t=1cm$ into (4) yields $C=3mF$. Figure 4 shows the proposed low pass filter where R depicts the equivalent resistance of the lumped inductor, L depicts the planar inductor and C that of interdigitated capacitor.
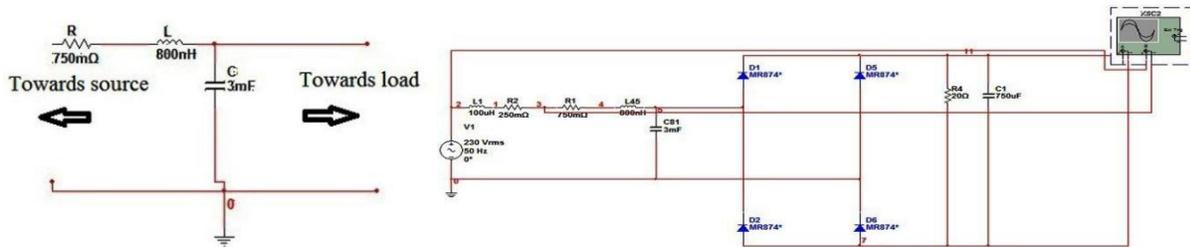

Figure 4 Diode bridge rectifier with designed planar low pass Filter

Figure. 4 shows the nonlinear diode bridge rectifier load with designed planar filter. The designed filter with giant dielectric constant material can withstand the power rating of the load. In this work the low pass filter is designed with cut off frequency of 75Hz so that the harmonic orders from three onwards are removed from the system. The qualitative analysis of the single phase bridge rectifier on including the above mentioned proposed filter is simulated using Multisim software on taking into account the temperature dependent resistance of the silica strip also.

The insertion loss for the proposed filter is observed to be 0.455 dB confirming the negligible power loss incurred by the same. TABLE II displays the harmonics distortion level of single phase diode bridge rectifier for various values of the load parameters on employing the proposed filter. Fig. 5 shows the bode plot of the designed planar low pass filter which shows that the cut off frequency of the proposed filter is 75Hz as a result of which higher order harmonics other than fundamental frequency are removed from the system. This forms one of the main results of the present work. Fourier analysis of Input current with filter is shown in Fig. 6 where the total harmonic distortion is reduced well within the IEEE standard 519-1992 of 5%. On carrying out a detailed analysis of the proposed filter system, it can be observed that the Total harmonic distortion (THD) of diode bridge rectifier is considerably reduced. This is also evident from the input voltage and current waveforms shown in Fig. 6.
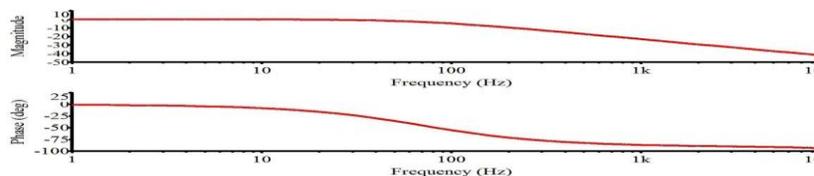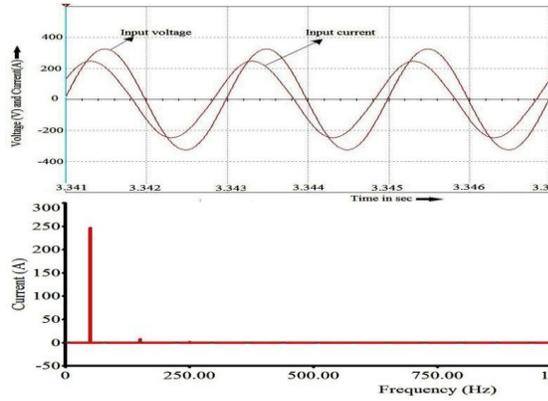

Figure 5 Frequency response analysis of designed planar Filter

THD = 1.9741% , Number of Harmonics =20, DC component = 0.0002

Har. Orde	Frequ ency	Magnitu de	Phase	Norm. Mag	Norm. Phase
1	50	244.55	-150.26	1	0
2	100	0.00189	-0.7219	7.73e-005	149.538
3	150	4.60569	140.34	0.01883	290.564
4	200	0.00086	115.44	3.55e-006	265.703
5	250	1.15331	-169.4	0.004716	-19.14
6	300	0.00031	-150.92	1.29e-006	-0.6612
7	350	0.80116	-58.518	0.003276	91.7422
8	400	0.00065	-49.76	2.66e-006	100.5
9	450	0.28062	49.483	0.001147	196.744
10	500	0.00049	113.81	2.02e-006	264.078
11	550	0.16552	135.75	0.000675	286.017
12	600	0.00012	-120.17	5.15e-007	30.0942
13	650	0.10831	-96.961	0.000442	53.2993
14	700	0.00054	-66.946	2.22e-006	83.314
15	750	0.04018	32.567	0.000164	182.828
16	800	0.00064	120.03	2.64e-006	270.29
17	850	0.03232	131.18	0.000132	281.44
18	900	0.00010	-54.343	4.33e-007	95.917
19	950	0.03211	-90.489	0.000131	59.77
20	1000	0.00023	-70.063	9.55e-007	80.1969

Figure 6 Waveform, Spectrum and THD analysis of diode bridge rectifier without filter

The input current wave form retains its sinusoidal nature (as is evident from Fig. 6) after the inclusion of the proposed filter in the input side.

TABLE I COMPARISON OF THD WITHOUT WITH DESIGNED FILTER

Load parameters	Without filter (%)	With Filter (%)
R_{load}=10 ohm and C_{load} = 220 µF	52.85	1.97
R_{load}=10 ohm and C_{load} = 470 µF	50.85	2.07
R_{load}=10 ohm and C_{load} = 740 µF	48.59	2.38
R_{load}=20 ohm and C_{load} = 220 µF	54.63	2.84
R_{load}=20 ohm and C_{load} = 470 µF	52.82	2.94
R_{load}=20 ohm and C_{load} = 740 µF	52.70	3.09
R_{load} =32 ohm and C_{load} = 220 µF	55.59	3.21
R_{load} =32 ohm and C_{load} = 470 µF	54.56	3.33
R_{load} =32 ohm and C_{load} = 740 µF	68.30	3.44

C. Analysis of Load Parameter Variation

The simulation of the proposed filter is further carried out by performing the frequency response analysis when the load capacitance C_{load} value is dynamically varied from 1µF to 1000µF for a given load resistance R_{load} at 20 ohm and is depicted in Fig. 7. It can be inferred that the low cut-off frequency of the proposed filter remains unaltered even after varying the load capacitance values. It is further observed from Fig. 7 that the low cut-off frequency value of the proposed filter does not change even after dynamically varying the load resistance values from 10Ω to 100Ω for a given value of C_{load} at 220µF.

The frequency response of the designed filter is also shown in Fig. 7 when the source inductance is varied from 1mH to 10mH. One can infer that the variation in the source inductance does not alter the frequency response of the proposed filter except the small change in the roll off rate of the proposed filter. Finally, the proposed filter is subjected to a rigorous test by analyzing the variations in the cut-off frequency of the low pass filter by changing the lumped inductance and lumped capacitance values of the same.

There is a possibility for the Inductance value of the proposed filter to change owing to aging. On varying the inductance value of the lumped inductor from 800nH to 1mH of the proposed filter, it is observed that the cut-off frequency of the proposed low pass filter does not change as is evident from Fig. 7. This throws light on the fact that the detuning effect due to variation in the proposed inductance value has only

a infinitesimal effect on the filter performance. Owing to the enormous dielectric constant value of the interdigitated capacitor of the proposed filter, the capacitance value of the same is not liable to change. This guarantees the robustness of the cut-off frequency of the proposed low pass filter for a given interdigitated capacitor design [12], [22], [23]. As is evident from (4) the capacitance value of the interdigitaed capacitor of the proposed filter can be changed by changing the number of fingers N present in the design. It is evident from Fig. 7 that the cut-off frequency values of the proposed low pass filter changes with the change in the capacitance value. Hence one can emphasize that the proposed low pass filter can be tuned to any appropriate frequency.
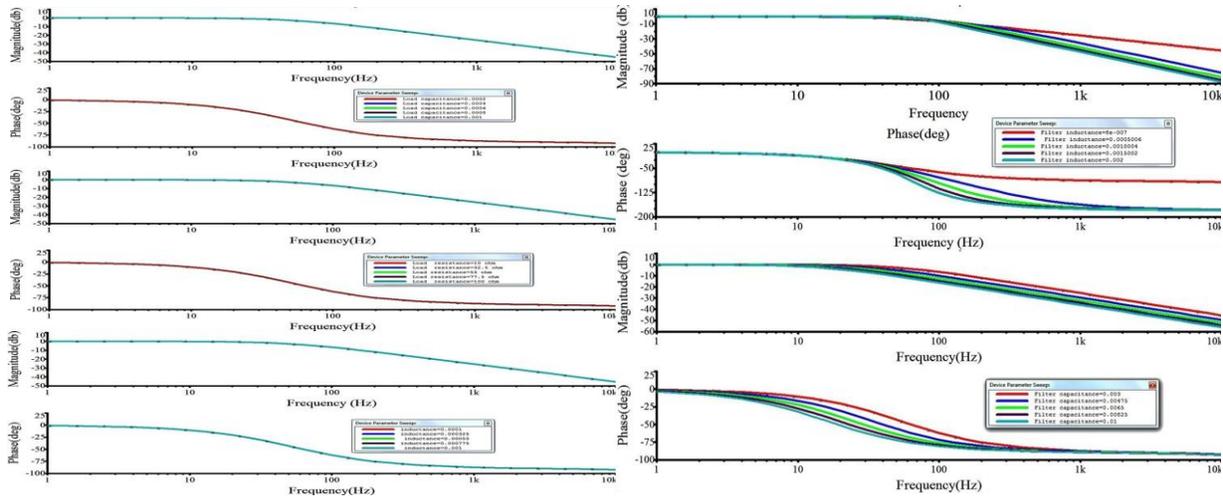

Figure 6 Parametric Analysis of Filter Cutoff with respect to load capacitance (left top), load resistance (left middle), source inductance (left bottom), filter inductance (right top) and filter capacitance (right bottom)

4. Conclusion

In this paper a low loss passive filtering technique using voltage source type nonlinear load with the single phase diode bridge rectifier as a benchmark circuit comprising of high impedance line inductor and interdigitated fractal capacitor is proposed. The high impedance line inductor is made of fused silica and hence is characterized by time varying temperature dependent resistance. The highlight of the designed high impedance line inductor is the negation of any dynamic impedance changes in the nonlinear load. The interdigitated fractal capacitor is made of $La_{0.5}Na_{0.5}Cu_3Ti_4O_{12}$, a giant K dielectric material, thereby being instrumental in contributing to a comparatively large capacitance value of the order of 3mF with a reasonably small size. Spice based simulation and subsequent analyses revealed a wide stop band range with 3db cut-off at 75Hz. Hence multiple higher order harmonics are effectively eliminated by using a single filter over the entire wide band. Moreover, the extensive simulation also pointed out low insertion loss for the proposed filter. It has been observed that even in spite of dynamic load variation, the designed filter is able to keep the THD of the supply current well below the limit specified by the IEEE 519 -1992 standard. The proposed low pass filter pertains to the elite realm of smart filter by fulfilling the golden standards of low loss, low distortion, easy tunability and small size simultaneously.

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