Photonic Crystal Return-to-Zero NAND Gate in the visible spectrum

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Abstract

A simplified photonic crystal design for an all-optical NAND gate operating in the visible spectrum is proposed and validated with numerical experiments using Finite Difference Time Domain method. Considering the NAND gate as a optical four-port network, the scattering matrix is determined. Also, two-dimensional autocorrelation-based leakage analysis is done and temporal analysis of the output pulse is performed. From the above mentioned valuations, one can obtain the optimal performance of the NAND gate structure with minimal loss and distortion, which forms the novelty of the present work.

Keywords: Photonic Crystals, All optical NAND Gate, Pulsed Logic Gates, Photonic Bandgap, FDTD

1. Introduction

With the advent of very large Scale integration (VLSI) and optical microlithographic fabrication techniques, miniaturization and mass production of planar optical elements made up of microscopic structures have made it possible for optical technology to make a metamorphic leap from analog optics to digital optics [1]. Moreover, the initiation of digital diffractive optics, digital waveguide optics, or their combination, have further paved the way for new or improved optical functionalities, thereby opening the doorway for a plethora of applications, ranging from optical data storage to biophotonics [1, 2]. Among the various types of diffractive optics, sub-wavelength diffractive optics stands in the forefront owing to its high-speed processing capabilities. As the basic structures of these sub-wavelength diffractive elements are much smaller than the wavelength of the photonic signal, they are also known as nano-optical elements [5]. Among them, photonic band-gap based nano-optical elements, also known as photonic crystals [3], dominate the all-optical signal processing platform owing to the abrupt changes in their refractive index profiles and hence, their polarizations [4]. Based on their confinement of light, photonic crystals can be broadly classified as one-, two-, and three-dimensional [6]. Examples of one dimensional photonic crystals include fiber Bragg gratings [7]. Two-dimensional photonic crystals include photonic crystal fibers and planar photonic crystal waveguides [8] whose diverse applications include all optical switching devices[9], lasers [10] and slow-light guiding [11]. Woodpiles fall under the category of three dimensional photonic crystals [12, 13]. The present paper purports the designing and operation of all-optical NAND gates using two dimensional photonic crystals.

Logic gates form the basic units of digital computing and signal processing. Extensive research work has been carried out both theoretically and experimentally, in all-optical logic gates employing photonic crystals, as they offer tremendous switching speeds [14, 15, 16], albeit employing complicated defect arrangements. Further, the above mentioned gate designs use continuous wave logic (Non-Return to Zero pulses), and often use light in the far Infrared region of the electromagnetic spectrum . Similar all-optical logic operations can also be brought about by innovative engineering of the defects thereby manipulating the flow of visibe light. Based on a simplified arrangement of defects, with the host material being silicon, the optical functionality of NAND logic is theoretically analyzed and validated with numerical experiments in this present work with optical Gaussian pulses (Return to Zero Logic) as input. The optimal performance of the all-optical NAND gate characterized by minimal leakage and negligible distortion with the arrangement of defects designed in a simplified manner and hence which can lead to easy experimental realization, form the major results of this work.

2. Design of all optical NAND gate

In the photonic band-gaps of photonic crystals in general, certain wavelengths of light are forbidden to pass through a periodically designed structure, and these are analogous to electronic band-gaps in this regard [7]. By careful selection of the photonic band-gap, and hence the lattice dimensions and the operating wavelengths, suitable guiding and directional

manipulations of light can be achieved in an effective manner [7]. Based on the above mentioned fact, in the present work, the basic lattice structure is designed as a square-lattice using silicon rods with dielectric constant $\varepsilon = 12$ in air, with the rods having a radius $r = 60nm$ radius and the lattice unit or the rod spacing being $a = 500nm$. Experimental fabrication of lattice structures with sub-100nm radius has been reported in [17].

In the absence of sources, the Maxwell's equations for simple isotropic dielectric material are given in [18]. Fully - vectorial eigen modes of the Maxwell's equations with periodic boundary conditions are computed by preconditioned conjugate miniaturization of the block Rayleigh quotient in a planewave basis using MIT's open-source package MPB (MIT Photonic Bandgap) [18].

The band-gap diagram, which portrays the dispersion relation between angular frequency ω and the wave vector k is as shown in Fig.(1). One observes a significant band-gap between band 1 (corresponding to $\dfrac{a}{\lambda}$ of 0-0.38) and band
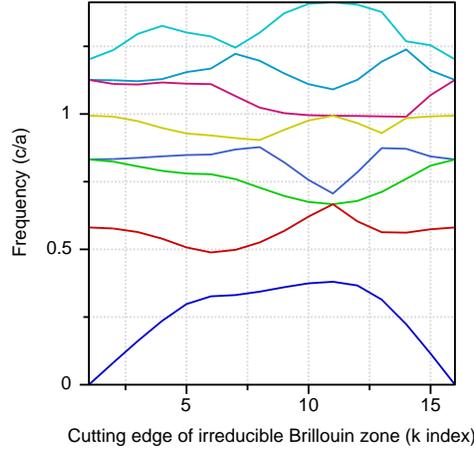

Figure 1: Photonic Band-Gap Diagram

2(corressponding to $\dfrac{a}{\lambda}$ of 0.48-0.55), where the propagation constant k_z has a value of 11. The structure operates at the band-gap corresponding to $\dfrac{a}{\lambda}$ value of 0.4, where "a" is the lattice constant and λ are the appropriately available operating wavelengths which are obtained as $\lambda_1 = 400nm$ and $\lambda_2 = 380nm$ in the visible region, corresponding to the violet regime.

The designed structure has simple line defects that act as waveguides for the above mentioned wavelengths in the band-gap. The basic length parameters for the proposed NAND gate are $L_1 = L_2 = 14a$, $L_3 = 11a$ and $L_4 = 32a$. These basic lengths are chosen so as to introduce a phase difference of 180°. The phase delay of propagation through the lengths L_1, L_2, L_3 and L_4 can be described using the expression:

$$
\begin{aligned}
\phi_1 &= \left(\frac{2\pi L_1 a}{\lambda_1} \right) + \pi = 12.51\pi, \\
\phi_2 &= \left(\frac{2\pi L_2 a}{\lambda_1} \right) = 11.51\pi, \\
\phi_3 &= \left(\frac{2\pi a \left(L_1 + L_4 \right)}{\lambda_2} \right) + \pi = 24.77\pi \text{ and} \\
\phi_4 &= \left(\frac{2\pi L_3 a}{\lambda_2} \right) = 8.52\pi.
\end{aligned}
\tag{1}
$$

Based on these calculations, the structure is proposed for NAND gate. The geometry of the simple line defect structure is defined using the option of "polygons" available in the package Python-Meep [19] and is portrayed in Fig.(2).

3. Results and Discussions

The input signal is selected to be a Gaussian pulse with a FWHM pulse width of 150fs. Here, the two inputs A and B are launched from the two ports labeled "Input A" and "Input B" as shown, and the output is taken from the port labeled "Output". The other port labeled "Reference" is also an input port where a pulse of wavelength λ_1 and another of wavelength λ_2 are launched together. The output logic value is determined by the presence of a pulse (high) or the
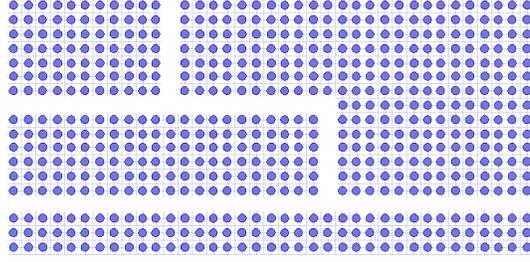
Figure 2: Structure of NAND Gate as obtained from the Python-Meep simulation on employing the option of "polygons"

absence of a pulse (low). Hence a threshold of 0.5×10^{-5} is set at the output port, this threshold being set in order to allow for negligible leakage. Any value above this threshold corresponds to a logic high ("1") and below this is a logic low ("0"). Appropriate input values are given, and the corresponding outputs are obtained and are verified with respect to the truth table of NAND gate. In order to observe the flow of the Gaussian signal through the defect, a contour plot obtained by adding the field intensities over all timesteps, is depicted in Fig.(3).
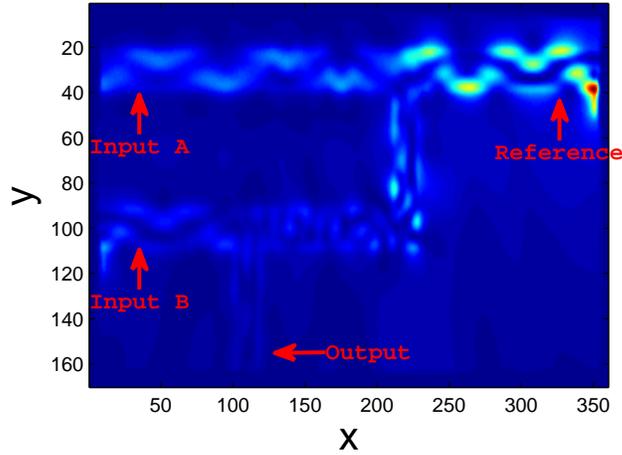

Figure 3: Contour plot over all timesteps, showing the flow of light, for A=0,B=1

Figure (4) shows the surface plot taken at the final sampling instant (i.e when all input sources have decayed), and shows the field intensity that would be obtained by a detector at the output port as a logic high or low depending upon the fixed threshold value.

In a similar manner, the corresponding output surface plots for the cases $(A = 0, B = 0)$, $(A = 1, B = 0)$ and $(A = 1, B = 1)$ are portrayed in Figs.(5)-(7). Hence, from all the above surface plots, one can infer that the NAND logic operations are obtained exactly as desired.

Considering Input A as port 1, Reference as port 2, Input B as port 3 and the Output as port 4, an optical four port network can be perceived and hence the portwise performance of this optical network can be analyzed in the form of a matrix equation which is given by the relation

$$[Y] = [S][X], \tag{2}$$

where the column matrix represented by $[X]$ is the input power matrix with X_i $(i = 1 \cdots 4)$ are the input powers. In a similar way, the column matrix represented by $[Y]$ is the output power matrix with Y_i $(i = 1 \cdots 4)$ are the output powers. Moreover, the square matrix $[S]$ of order 4 is the optical scattering matrix which brings out the port-wise performance of the optical NAND gate and the matrix elements S_{ij} of the scattering matrix $[S]$ are given by the relation

$$S_{ij} = \left. \frac{Y_i}{X_j} \right|_{X_k=0, \ k \neq j}. \tag{3}$$

Here, the diagonal elements S_{ii} of $[S]$ represent the reflection coefficients of the port "i" and the corresponding off-diagonal elements S_{ij} represent the transmission coefficients from port "j" to port "i" of the optical four port network.
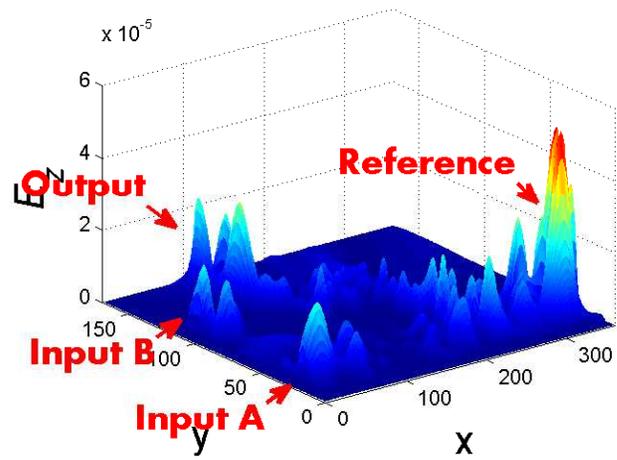
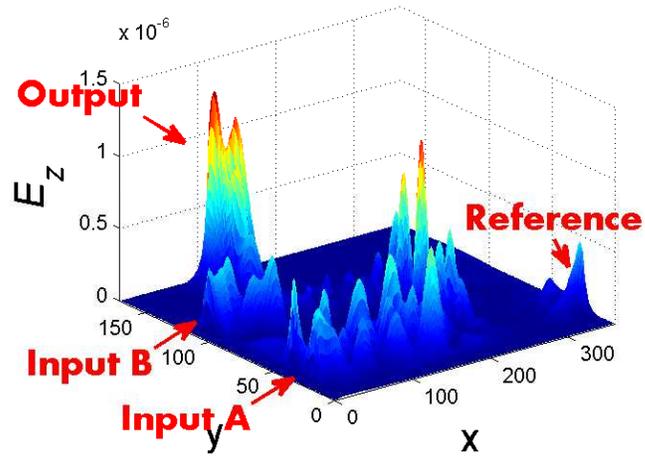3

Figure 4: Surface plot at final timestep for A=0,B=1

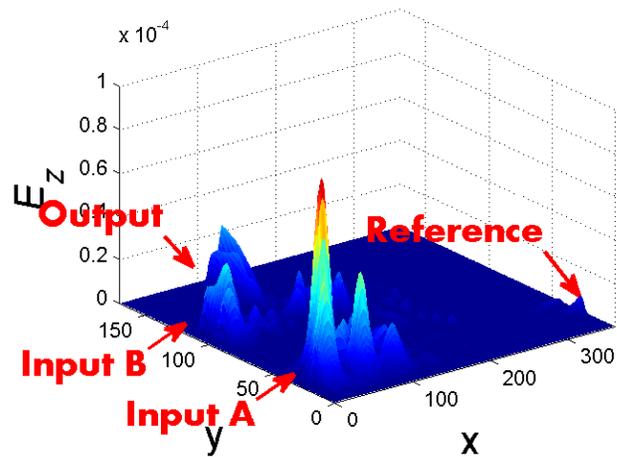Figure 5: Surface plot at initial timestep for A=0,B=0

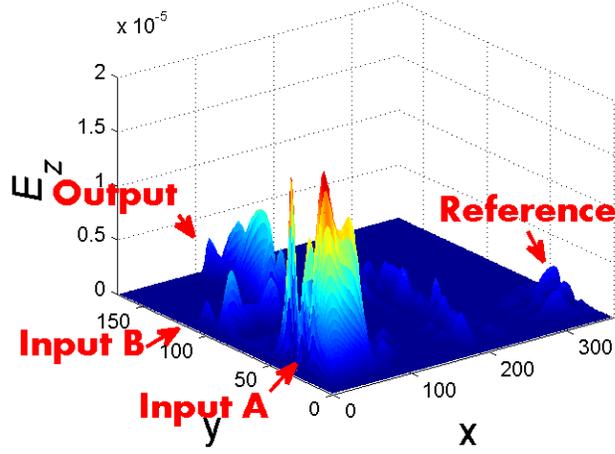Figure 6: Surface plot at initial timestep for A=1,B=0

4

Figure 7: Surface plot at initial timestep for A=1,B=1

From the surface plots given by Figs.(4)-(7), the numerical elements of the scattering matrix elements S_{ij} are calculated from Eq.(3) and hence are obtained as follows:

$$[S] = \begin{pmatrix} 0.6 & 0.05 & 0.1 & 0.05 \\ 0.9 & 0.9 & 0.7 & 0.4 \\ 0.4 & 0.05 & 0.05 & 0.05 \\ 0.9 & 0.3 & 0.7 & 0.1 \end{pmatrix}. \tag{4}$$

From Eq.(4), one can judge the port-wise performance of the optical NAND gate. Of special mention are the transmission coefficients from inputs ports A and B to the output port i.e. $S_{41} = 0.9$ and $S_{43} = 0.7$, which have high values, in contrast to the corresponding backward propagation coefficients $S_{14} = 0.05$ and $S_{34} = 0.05$.

Furthermore, the leakage throughout the NAND gate structure is characterized by performing a two-dimensional autocorrelation trace which is plotted in Fig.(8).
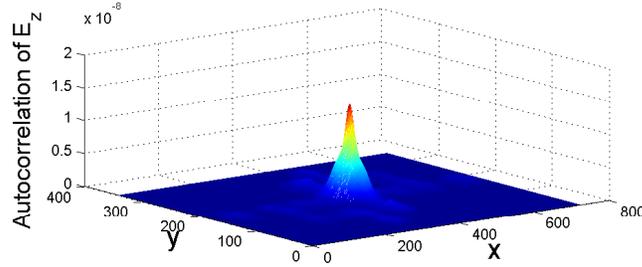

Figure 8: Two-Dimensional Autocorrelation

On analyzing the obtained surface plot, one can very much infer that the leakage is minimal throughout the NAND gate structure, owing to the high contrast observed between the autocorrelation at the center and autocorrelation values at other locations.

The output pulse is portrayed in Fig.(9). Here the pulse amplitude is plotted as a function of time-step, each time-step being equal to 5fs. The FWHM observed is 150fs, well in agreement with the proposed design.

4. Conclusion

From the above mentioned detailed analysis, one can validate the optimal performance of the entire NAND gate structure with minimal loss and distortion, which forms the main result of the work. Also, since Return-to-zero (RZ) pulses are employed for performing logic operations, high bit rates can be achieved. Since NAND gate is one of the universal logic gates, it forms the fundamental building block for many digital components including both combinatorial
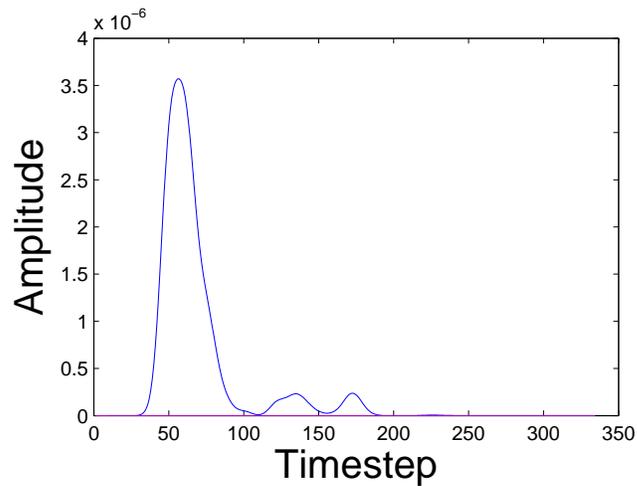
Figure 9: Output Pulse in time-domain. Here 1 Timestep = 5fs

logic elements such as multiplexers, encoder-decoders and arithmetic-logic units(ALU), and sequential logic elements such as flip-flops, counters, registers and read-write memories. Hence, future work points to designing such logic elements, by appropriate NAND gate combinations.

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