Quantum Computation using Chaos based S-Bits

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Abstract
The present work purports to the proposal and elucidation of a novel kind of logic, where the apparent 'practical uncertainty' of chaos is effectively harnessed in the form of S-Bits, or Simultaneous Bits, to achieve quantum computation like effects. Specifically, it is seen that a single NMOSFET possessed the sufficient nonlinearity to generate a signal driven chaos, which is then proposed as similar to the superposed state of a qubit, and hence termed "S-Bits". The measurement/collapse operations are performed using hysteresis, achieved using back-to-back MOS Varactors. Using these formulations, various quantum and reversible logic gates such as the three Pauli Rotation Gates, Hadamard Gate, CNOT and TOFFOLI gates are implemented in hardware level using extremely simple circuitry. Following this, the phenomenon of entanglement using S-bits is discussed, followed by implementations of quantum teleportation and superdense coding. The results reveal the effective reproduction of quantum computation applications using simple circuitry involving the S-Bit analogue, thus ushering in the golden era of affordable quantum computing.

1. Introduction
The current era of information technology has certainly taken the world by storm with the development of cloud computing and Big Data Systems having enabled humongous amounts of storage [1-2]. However, a very critical concern arising out of current information processing and storage technology is that of security, with a lot of news filled with despairing stories of hacking and cyber security violations [3]. A lot of effort is thus being put in using the principles of information theory to find out effective ways of increasing information security and processing speed, with one of the most popular solutions being Quantum Computing [4-5]. The concept of quantum bit (Qubit), which is based on the fundamental principle of uncertainty, enables processing of multiple bits simultaneously, drastically increasing the speed [5].

A lot of literature exists, pertaining to the proposal and experimental implementation of quantum computing based on many aspects of physics, some of the noteworthy being Superconducting Systems, Nuclear Magnetic Resonance, Spin based systems and Cavity Quantum Electrodynamics [6-10]. These implementations are however fraught with limitations and difficulties in implementation such as the requirement of cryogenic conditions, high magnetic fields, lattice fabrication difficulties and so on [6-10].

The present work purports to the design and implementation of a Qubit-like system of superposed logic levels by effectively harnessing nonlinear principles. Specifically, the present work uses the nonlinearity of Metal Oxide Semiconductor (MOS) transistor devices to generate chaos and also use the principles of entanglement to achieve a state of parallel processing similar to that of the quantum bit. Various classical

and quantum logic gates using these principles are then demonstrated. The extreme simplicity of the circuit combined with the effective usage of nonlinearity to harness the power of parallel computing form the novelties of the present work.

2. Methodology

The obkective of the present work is to create a parallel computing state reminiscent of a Qubit, and to demonstrate basic logic gates using the same. The logic assumed in the present work is positive non return to zero (NRZ) logic. The computing system consists of three stages:

1. Creating a superposition state.
2. Performing the logical operations using the superposed states.
3. Separation of the superposed states.

A. Creating a Superposition State

This stage is similar to the process of preparing the qubits in a quantum computer. Since level logic is assumed, logical '0' is Ground (0V), and logical '1' is the Supply Voltage Vdd (V). Thus if Vdd is 1V, then we have |0> = 0V, and |1> = 1V. Any voltage level in between 0V and 1V can thus be viewed as a superposition of the two states. For example, 0.7V corresponds to 0.7|1>+0.3|0>. Thus, the 'superposed' state is merely any state lying in between 'pure' 1 (0|0>+1|1>) (1V) and 'pure' 1 'pure' 0 (1|0>+0|1>) (0V).

One of the significant hallmarks of a quantum bit is the uncertainty concept, which enables the bits to take the superposed states. In other words, during measurement, the superposed state collapses into one of the two 'pure' states and until that point in time, the result is uncertain. This uncertainty can be viewed as the resultant of the complexity of the system. In the present work, the complexity, and hence, the apparent illusion of 'uncertainty' is achieved using chaos theory, a defining highlight of twentieth century physics with the characteristic signatures of determinism and sensitive dependence on initial conditions [11-14].

The fundamental criterion to generate chaos is nonlinearity. In the present work, the nonlinearity of a semiconductor device such as a MOSFET, inferred from the output characteristics is used to generate chaos [15-16]. This nonlinearity mainly arises due to the non quasi static operation of the channel, and the nonlinear behavior can be understood by the nonlinear transmission line representation of the channel [17-18]. This channel nonlinearity also affects the current voltage relationship of a MOSFET, with the Drain Current of a MOSFET nonlinearly dependent on the gate and drain voltages.

Thus, in order to generate chaos, two signals are given to the gate and drain terminals of an n-MOSFET and the output is taken from the source terminal, as illustrated in Fig. 1.

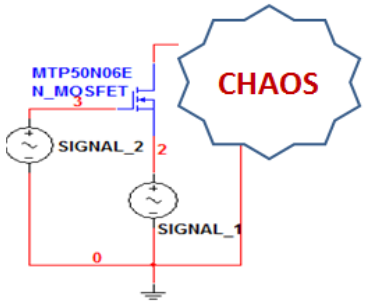

Figure 1 Generation of Chaos using single N-MOSFET

The above mentioned principle is experimentally validated. The gate and drain signal amplitudes are set to 2Vrms and 5Vrms respectively. The gate signal frequency is set to 1MHz. By altering the drain frequency and thus the gate to drain frequency ratio, the stability and complexity of the single nMOS system is altered. The phase portraits of the generated signals reveal that at various ratios such as 1:2, 1:3 and 1:4, 2, 3 and 4 loops are seen respectively, corresponding to period doubling, tripling and quadrupling. At suitable non-integral ratio such as 1:2.9, chaos is generated. The phase portraits obtained are shown in Fig. 2.

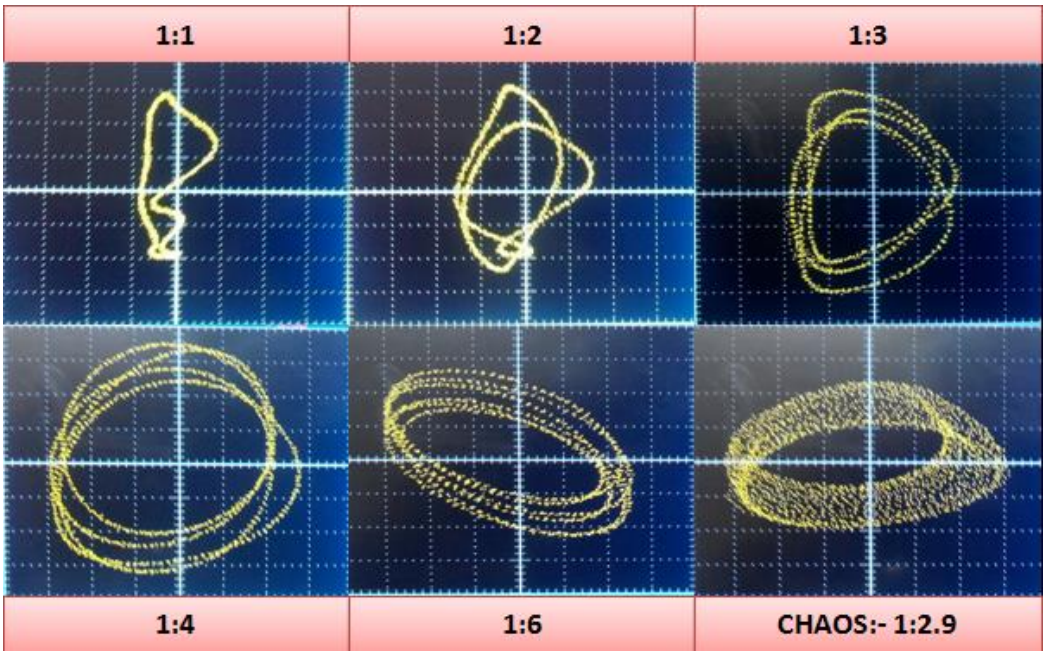

Figure 2 The 'Road to Chaos' using Single N-MOSFET

In order to make the signal more conducive to representing logic states, the drain input is replaced with a square wave. A prototype superposed state is generated with the resulting output signal in Fig. 3.

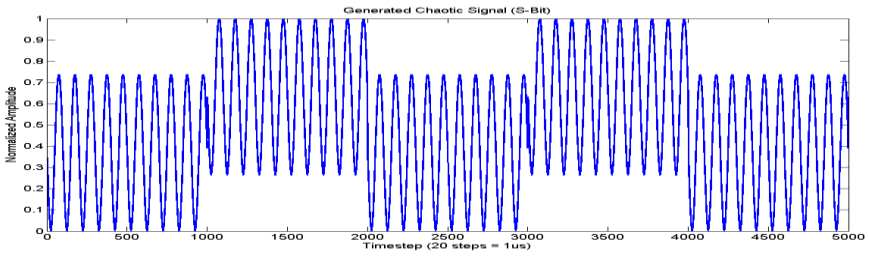

Figure 3 Generated Superposed State

In order to characterize the chaotic signal, nonlinear analysis is used. The Lyapunov exponent (LE) of the 1:2.9 chaotic signal is obtained as 27.92 using Rosenstein's algorithm, confirming its chaotic nature [19-20]. Also, the Kolmogorov entropy (K2) is obtained as 8 bits/symbol, highlighting the information content and the apparent "uncertainty" illusion of the generated signal [20]. As can be seen, the output signal is neither constantly at 1V nor at 0V. Thus, at any instant, this signal represents a superposition of the |1> and the |0> states. This property, coupled with the "uncertainty" seen in the K2 value yields the primary advantage of the Qubit – parallel computing, which can be explained using the concept of Bloch Sphere, where all points lying on the surface of the Bloch Sphere represent classical states of |0> or |1> and all points not on the surface represent 'mixed states' of |0> and |1>, which can be represented as superposition states of |0> and |1>. The generated chaotic waveform, representing the superposed states and reminiscent of the Qubit is termed the Simultaneous Bit or the "S-Bit".

B. Performing Logical Operations

The next stage is to perform logical operations using the generated S-Bits. Since the generated S-Bits conform to the NRZ level logic, conventional CMOS logic circuits can be used to perform classical logic gate operations on the S-Bits. In addition, reversible logic gates such as the Toffoli Gate, as well as Quantum logic Gates such as the Spin and Rotation gates can also be implemented using appropriate CMOS circuitry [5].

The outputs of a logical operation using superposed states typically consist of superposed states. For example, the operation of a Pauli X Gate, which is essentially an inverter (NOT Gate) is shown in Fig. 4.

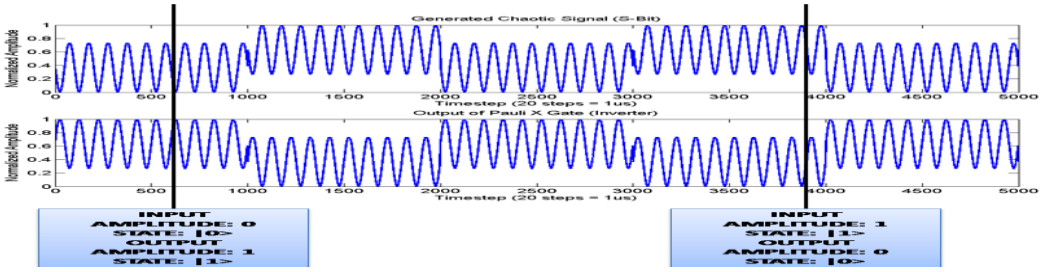

Figure 4 S-Bit Output of Pauli X/ NOT Gate

The Pauli Gate corresponds to a rotation of the Bloch Sphere around the X-axis by 180 degrees, mapping |0> to |1> and |1> to |0>, represented by the following matrix

$$X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$$

C. Separation of the Superposed States

This stage corresponds to the Measurement and Collapse stage of a Qubit. In this stage, the superposed states are separated into the native 1 and 0 logic levels, thus converting an S-Bit to a classical bit. In order to achieve the separation of states, voltage hysteresis is used. The voltage hysteresis can be achieved by connecting (in shunt) back-to-back MOS transistors at the output terminal. The back-to-back MOS transistors perform the function of back-to-back Varactors or Zener diodes, with each MOSFET setting a different threshold [21]. The result is that a voltage hysteresis loop is formed in between the two thresholds. The transfer plot of a CMOS inverter combined with a hysteresis element is shown in Fig. 5.

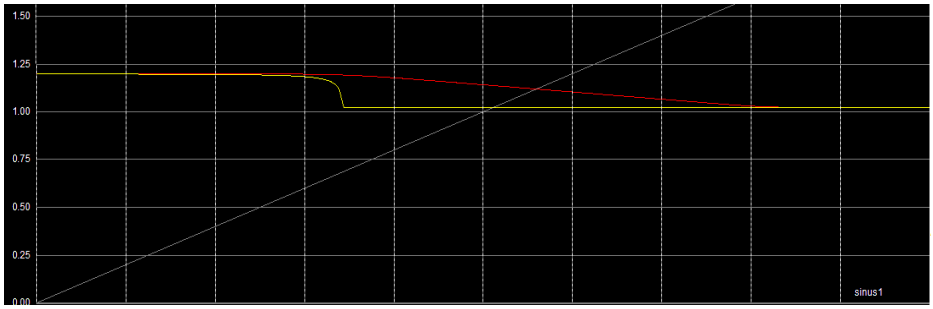

Figure 5 Voltage Transfer plot illustrating the voltage hysteresis

The output waveform obtained using hysteresis is shown in Fig. 6.

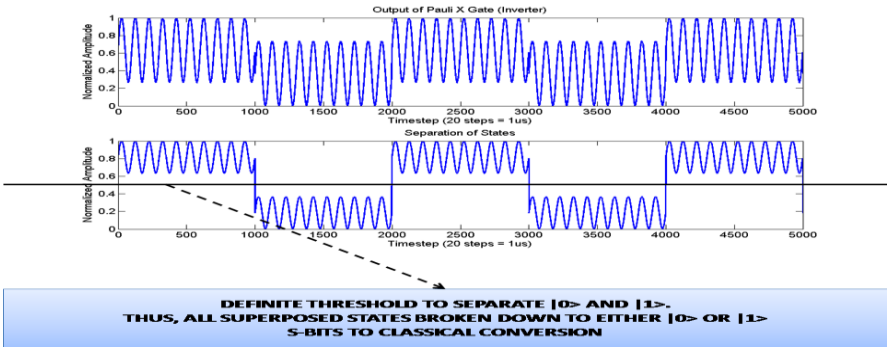

Figure 6 Output Waveform using Hysteresis showing the collapse of states

As can be seen, the hysteresis element enables the collapse of superposed states into two distinct levels, corresponding to |1> and |0>.

Thus, the above mentioned three stages for an S-Bit Pauli X Gate are highlighted as a schematic in Fig. 7.

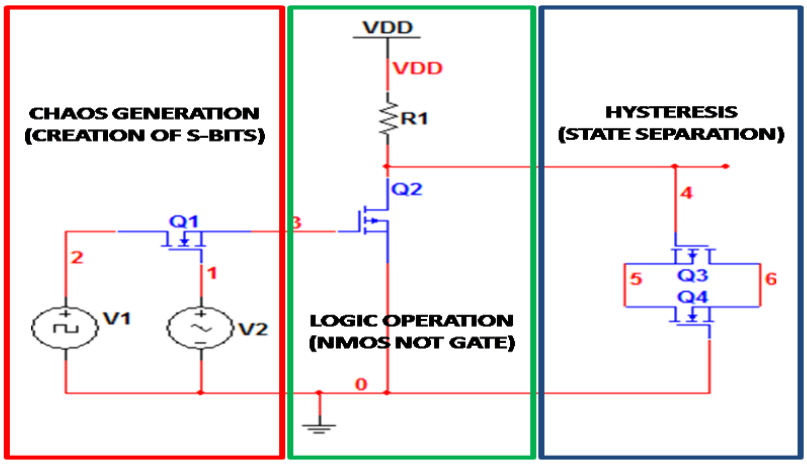

Figure 7 Schematic of S-Bit Pauli X Gate

Essentially, chaos generation corresponds to converting classical Bits to S-Bits and Hysteresis Element corresponds to converting S-Bits back to Classical Bits.

3. Results and Discussion

The three stages of S-Bit Generation, Logic Operation and Separation of States are implemented experimentally using chaos generation consisting of a single MTP50N06E transistor is used. The Drain signal is a square wave of amplitude 1.768Vrms and frequency 10kHz. The Gate signal is a sinusoidal signal of amplitude 3.4Vrms and frequency 238kHz.

A. Quantum Gates

Quantum Gates, interpreted in the quantum sense are operators satisfying the usual properties of being unitary and Hermitian which implies that application of the same gate twice yields back the input. These gates are visualized as matrices, which form the 'truth tables' for implementation using the S-Bits [5].

The Pauli X Gate is a rotation of the Bloch Sphere around the X axis by 180 degrees with |0> is mapped to |1> and |1> is mapped to |0>. The Pauli Y Gate corresponds to the rotation of the Bloch sphere by an angle of 180 degrees along the y-axis with |0> mapped to i|1> and |1> is mapped to –i|0>. The inclusion of 'i' in the output can be viewed in terms of the chaotic signal as a phase shift of 90 degrees. This is equivalent to shifting the sinusoidal input signal by 90 degrees before feeding it into the gate terminal of the MOSFET. The Pauli Z Gate is a rotation of the Bloch Sphere by 180 degrees around the z-axis, mapping |1> to -|1> while leaving |0> unchanged. The implementation of the Pauli Z Gate is simply a reversal in the polarity of the input S-Bit. The three gates with the schematic, matrix formulation and simulated and experimental results are illustrated in Fig. 8.

In the classical sense, the Pauli X, Pauli Y and Pauli Z gates correspond to the NOT gate, since the phase of the underlying signal is ignored while thresholding and separating the states. However, the same is not true in the quantum states, where the retention of phase is crucial [5]. In the present work, this is achieved in the Pauli Y Gate by shifting the phase of one of the transistor inputs. This phase shift is enabled due to the chaotic nature of the generated S-Bit signal and thus forms a unique feature of the present work.

As seen from the phase portraits in Fig. 8, the Pauli X and Z gates look similar since both pertain to reversal of the polarity/voltage levels (interpreted classically as the NOT Gate). The only difference between Pauli X and Pauli Z are the voltage levels – X reverses states in positive voltage whereas Z reverses state in negative voltage. However, the Pauli Y gate is different. Not only does it reverse the state, it adds a phase shift ('i' term in the Pauli Y matrix) by 90 degrees, corresponding to the quantum concept of spin. This is seen in the phase plane plot by the shift of the 'rhombus' to the right end of the phase portrait. Thus it can be concluded that the flexibility offered by chaos in the phase domain enables the implementation of quantum states therein.

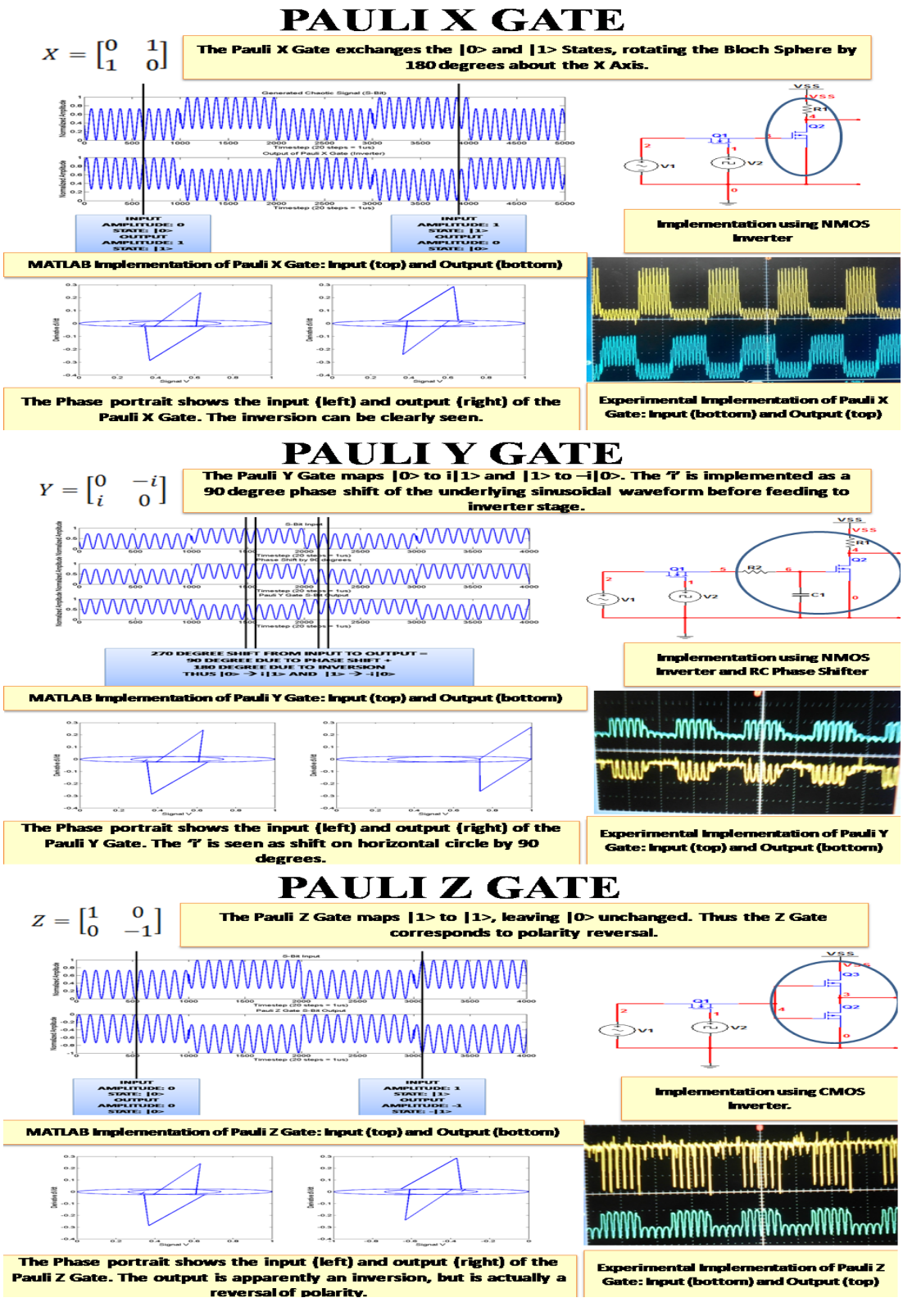

Figure 8 The Pauli X, Y and Z Gates for S-Bits

The Hadamard Gate is one of the fundamental quantum gates, derived from the unitary Hadamard Matrix. Functionally, the Hadamard gate maps |0> to 0.707(|0>+|1>) and |1> to 0.707(|0>-|1>). The matrix representation of the Hadamard Operator is as follows:

$$H = \frac{1}{\sqrt{2}}\begin{bmatrix}1 & 1\\ 1 & -1\end{bmatrix}$$

This gate can easily be implemented for S-Bit operations by first inverting the S-Bit, clamping it down from [1,-1] to [0.5,-0.5] and scaling the clamped signal by a factor of 1.414. The waveforms and phase portraits for S-Bit Hadamard gate are shown in Fig. 9.

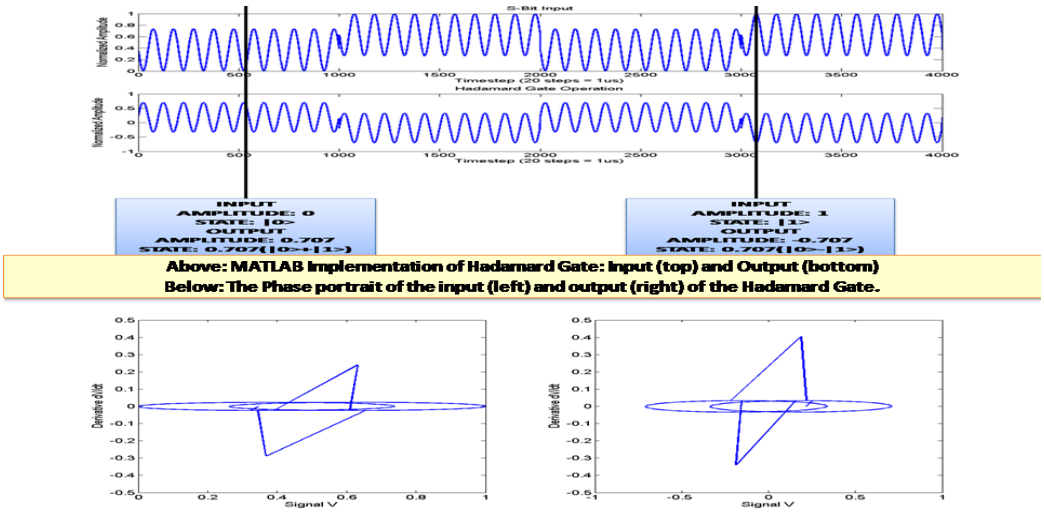

Figure 9 The Hadamard Gate

As can be seen, the Hadamard Gate transforms Pure States into superposition states. Thus it forms one of the fundamental building blocks for quantum computing. An interesting insight into the operation of the Hadamard Gate can be obtained when considering a mixed-state input. The output then becomes

$$\frac{1}{\sqrt{2}}\begin{bmatrix}|0>+|1>\\ |0>-|1>\end{bmatrix}\frac{1}{\sqrt{2}}\begin{bmatrix}1 & 1\\ 1 & -1\end{bmatrix} = \begin{bmatrix}|0>\\ |1>\end{bmatrix}$$

Thus, mixed states are mapped to pure states. Specifically, two mixed states interfere constructively to yield |1> and destructively to yield |0>. Thus, the Hadamard Gate corresponds to a specific and interesting case of Quantum Interference. This enables a lot of exciting applications such as Entanglement and Quantum Teleportation.

B. Reversible Gates

The CNOT Gate is the Controlled NOT Gate. The gate consists of two inputs, one of which acts as the control. The second input is inverted only if the control is at |1>. The control and the toggled input form the outputs, as illustrated in Fig. 10.

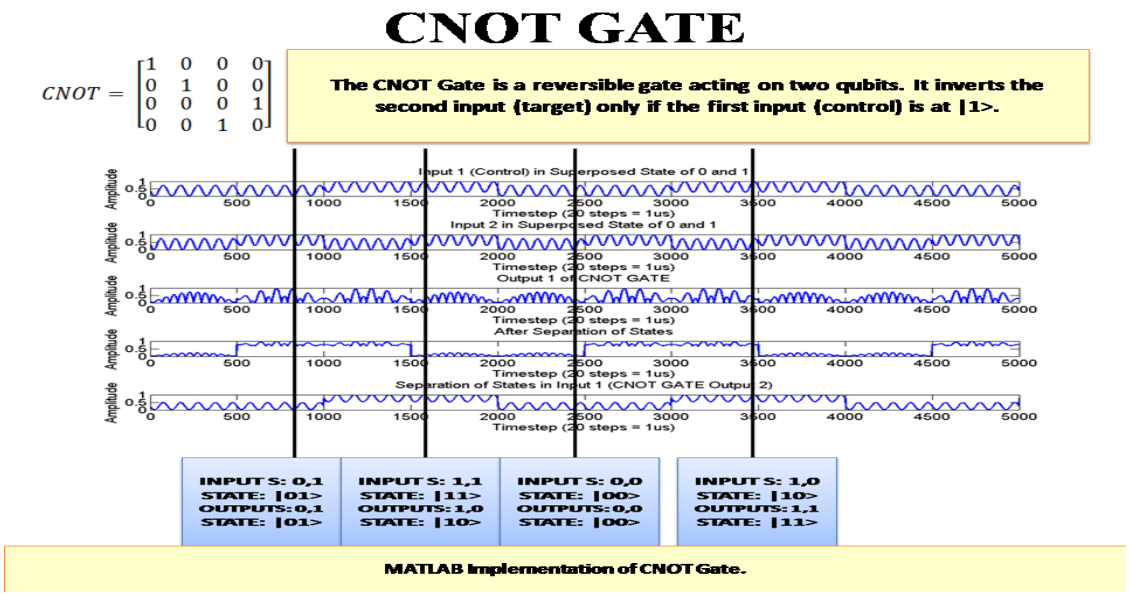

Figure 10 CNOT Gate using S-Bits

TOFFOLI Gate

The TOFFOLI Gate is a Controlled Controlled NOT Gate (CCNOT) and is a universal gate for classical computation. The Gate consists of three inputs, two of which are control. Only when both the control inputs are |1>, the third input toggles states. The two controls and the toggled state are returned as outputs.

$$TOFFOLI = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}$$

The waveforms of the TOFFOLI Gate are as in Fig. 11.

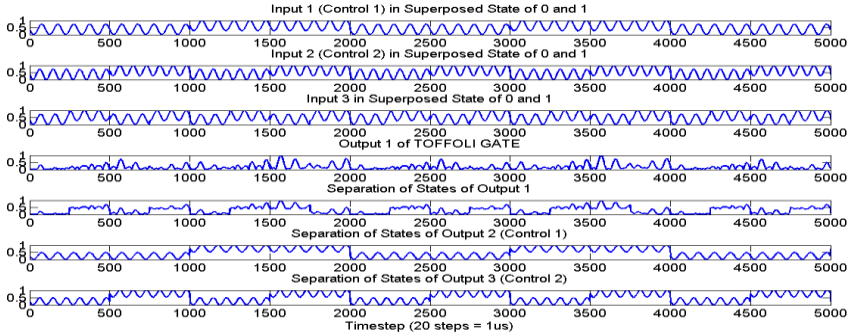

Figure 11 TOFFOLI Gate

4. Entanglement, Teleportation and Superdense Coding

One of the most fascinating applications of the Quantum Computing is in creating entangled states, which occurs when the phase relationship between two Qubits forces the observer to describe one particle in terms of another. In other words, any measurement made on one particle instantaneously affects the other. The most celebrated way of generating entanglement is by creating the Bell states. The Bell states for a two qubit system are given as follows:

|B00> = 0.707(|00>+|11>), |B01> = 0.707(|01>+|10>), |B10> = 0.707(|00>-|11>) and |B11> = 0.707(|01>-|10>)

The generation of the Bell states can be explained using a combination of the Hadamard and the CNOT gates. The schematic is shown in Fig. 12.

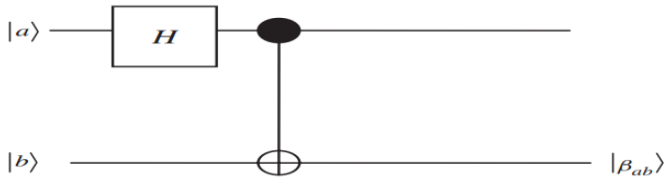

Figure 12 Generation of Bell States

By using the Hadamard gate, the first input is converted into the superposition form. This in turn, acts as a control for the CNOT gate, thus effectively 'imposing' its information onto the second bit. Thus the Bab (a,b=0,1) state is an entangled state, containing the information of a and b. The inputs and outputs of the Bell State Generation are shown in Fig. 13.

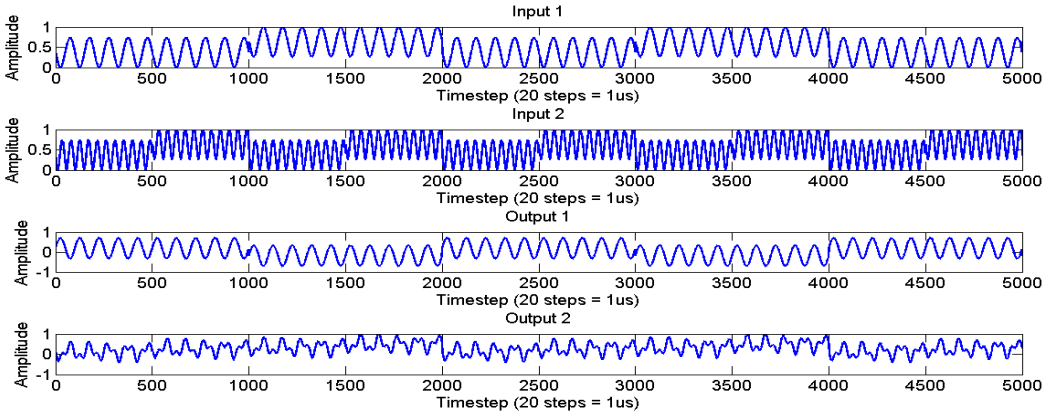

Figure 13 Generation of Bell States

The characteristics of the entanglement operation can be clearly visualized in the histograms and phase portraits of the inputs and the generated Bell State, shown in Fig. 14 and Fig. 15 respectively.

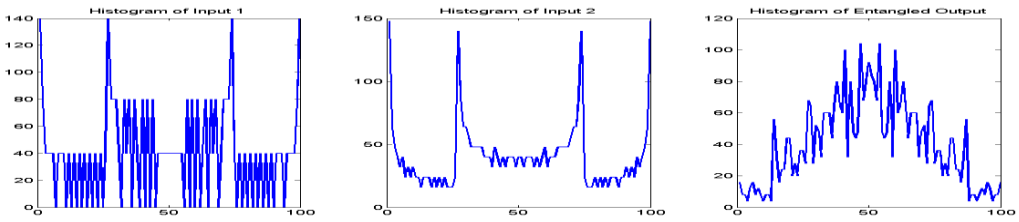

Figure 14 Histograms before and after entanglement

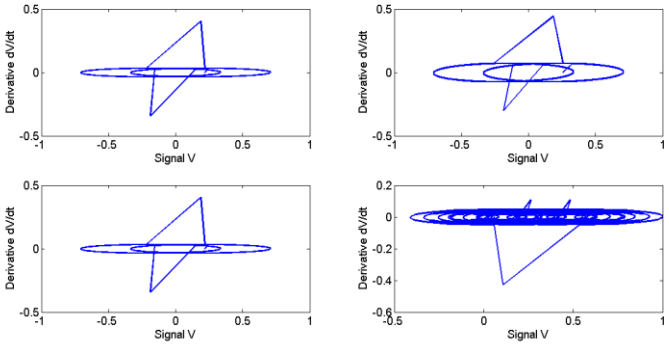

Figure 15 Phase Portrait of Bell State Generation Inputs (Top) and Outputs (Bottom)

An extension of the Entanglement process yields a rather fiction-like fantastical effect – Teleportation of Quantum Information – defined as transmitting a quantum state from one place to another without that state traversing the space in between. One bit quantum teleportation can be done using appropriate combinations of entanglement, CNOT, Hadamard, measurement and the Pauli X and Z gates. The schematic of one bit Quantum Teleportation can performed using a Pauli X gate is shown in Fig. 16.

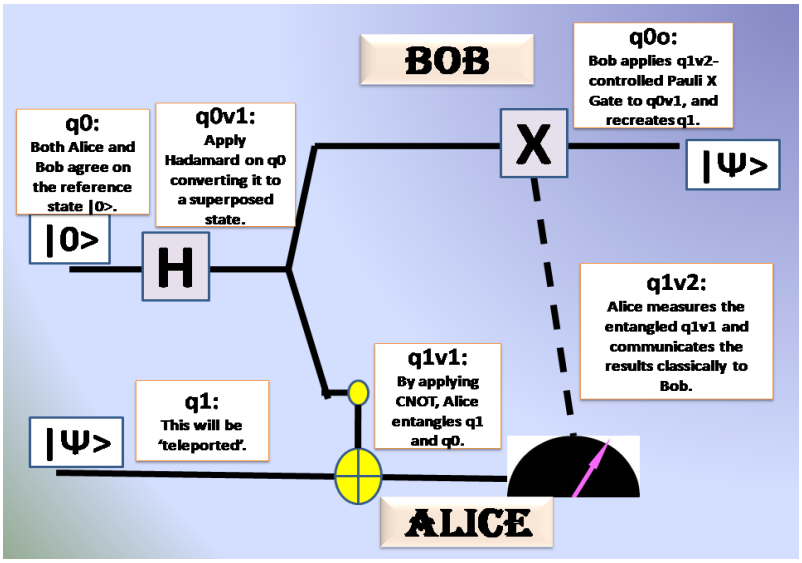

Figure 16 1 Bit Quantum Teleportation

Here, the objective is to transmit the qubit state of the second input to the first output i.e. q0o is the teleported version of q1. The waveforms of the original and teleported S-bit is shown in Fig. 17.

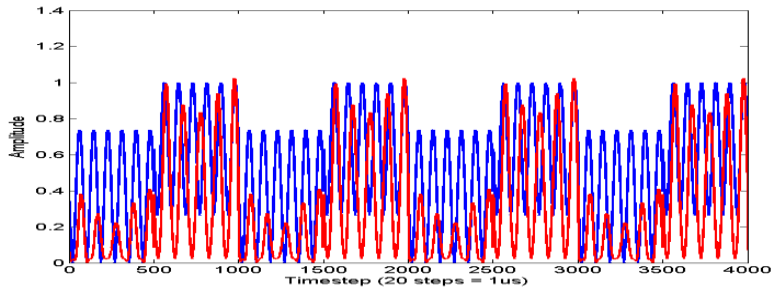

Figure 17 Waveforms of Input (Blue) and Teleported output (Red)

As is evident from the plot, the waveforms of q0o reasonably match the corresponding q1. This confirms that the quantum state has been teleported from node 2 to node 1 successfully. This also validates the implementation of entanglement since, quantum teleportation would not occur without successful entanglement and measurement.

Yet another fascinating application of the quantum computing world is that of superdense coding, where two bits are communicated through one single qubit. Thus, the long awaited promise of the qubit, the promise of "parallel" computing and communication can be achieved through superdense coding. The schematic of superdense coding is illustratedin Fig. 18.

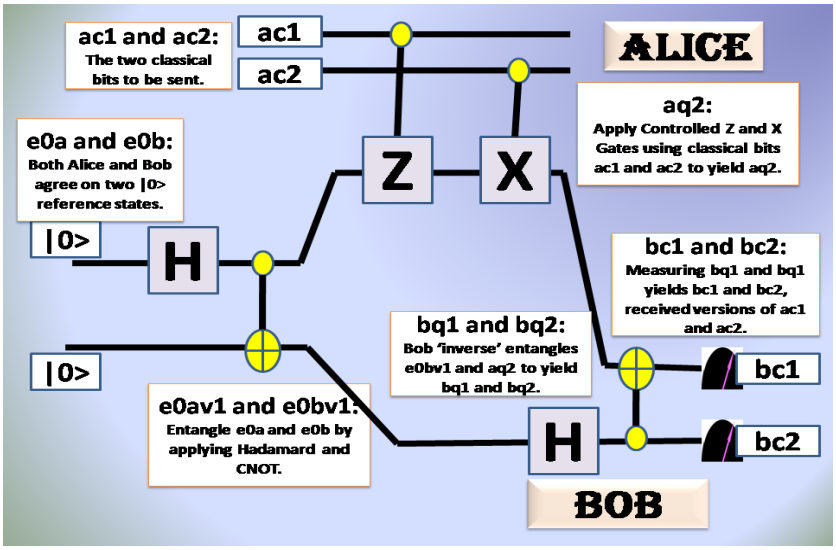

Figure 18 Superdense Coding

The objective here is to transmit two classical bits of Alice, ac1 and ac2 using a single qubit aq2 to Bob. Appropriate entanglement, Hadamard, CNOT and Pauli Gates enable Bob to measure aq2 yielding bc1 and bc2, received versions of ac1 and ac2. The transmitted and received waveforms of the two classical bits are plotted in Fig. 19.

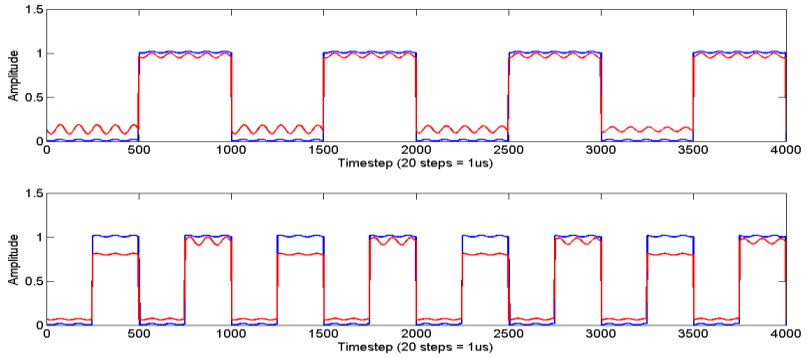

Figure 19 Transmitted (blue) and received (red) versions of the two bits

As seen, the transmitted and received versions of the two bits fairly match, confirming the suitability of the chaotic waveform to act as qubits demonstrating useful quantum computing applications.

5. Conclusion

The nonlinearity of the MOSFET has been effectively harnessed to generate chaotic signal. The chaotic signal, by virtue of its sensitivity, information content and flexibility in the phase domain provides a conducive platform to represent the superposition of logic states. This in turn, yields the advantage of parallel computing hitherto obtained only in quantum bits, and for this reason, the chaotic waveform has been christened the "S-Bit". Implementations of various classical and quantum logic gates have been performed at the system level, device level and experimentally using power transistors, extending the performance to quantum phenomena such as entanglement and quantum teleportation. The results reveal the effective implementation of quantum states and logic gates using simple circuitry involving the S-Bit, thus ushering in the golden era of affordable quantum computing.

References

[1] Armbrust, Michael, Armando Fox, Rean Griffith, Anthony D. Joseph, Randy Katz, Andy Konwinski, Gunho Lee et al. "A view of cloud computing." Communications of the ACM 53, no. 4 (2010): 50-58.
[2] McAfee, Andrew, Erik Brynjolfsson, Thomas H. Davenport, D. J. Patil, and Dominic Barton. "Big data." The management revolution. Harvard Bus Rev 90, no. 10 (2012): 61-67.
[3] Hansen, Lene, and Helen Nissenbaum. "Digital disaster, cyber security, and the Copenhagen School." International Studies Quarterly 53, no. 4 (2009): 1155-1175.
[4] Cavelty, Myriam Dunn. Cyber-security and threat politics: US efforts to secure the information age. Routledge, 2007.
[5] McMahon, David. Quantum computing explained. John Wiley & Sons, 2007.
[6] DiCarlo, L., J. M. Chow, J. M. Gambetta, Lev S. Bishop, B. R. Johnson, D. I. Schuster, J. Majer et al. "Demonstration of two-qubit algorithms with a superconducting quantum processor." Nature 460, no. 7252 (2009): 240-244.
[7] Jones, J. A., and M. Mosca. "Approximate quantum counting on an NMR ensemble quantum computer." Physical review letters 83, no. 5 (1999): 1050.
[8] Cummins, Holly K., Claire Jones, Alistair Furze, Nicholas F. Soffe, Michele Mosca, Josephine M. Peach, and Jonathan A. Jones. "Approximate quantum cloning with nuclear magnetic resonance." Physical review letters 88, no. 18 (2002): 187901.

[9] Földi, Péter, Balázs Molnár, Mihály G. Benedict, and F. M. Peeters. "Spintronic single-qubit gate based on a quantum ring with spin-orbit interaction." Physical Review B 71, no. 3 (2005): 033309.
[10] Imamog, A., David D. Awschalom, Guido Burkard, David P. DiVincenzo, Daniel Loss, M. Sherwin, and A. Small. "Quantum information processing using quantum dot spins and cavity QED." Physical Review Letters 83, no. 20 (1999): 4204.
[11] Strogatz, Steven H. Nonlinear dynamics and chaos: with applications to physics, biology, chemistry, and engineering. Westview press, 2014.
[12] Thompson, John Michael Tutill, and H. Bruce Stewart. Nonlinear dynamics and chaos. John Wiley & Sons, 2002.
[13] Ausloos, Marcel, and Michel Dirickx, eds. The logistic map and the route to chaos: From the beginnings to modern applications. Springer Science & Business Media, 2006.
[14] Bilotta, Eleonora, and Pietro Pantano. A gallery of Chua attractors. Singapore: World Scientific, 2008.
[15] Siligaris, Alexandre, Gilles Dambrine, Dominique Schreurs, and François Danneville. "A new empirical nonlinear model for sub-250 nm channel MOSFET." Microwave and Wireless Components Letters, IEEE 13, no. 10 (2003): 449-451.
[16] Hoile, G. A., and H. C. Reader. "Nonlinear MOSFET model for the design of RF power amplifiers." IEE Proceedings G (Circuits, Devices and Systems) 139, no. 5 (1992): 574-580.
[17] Chan, Mansun, Kelvin Y. Hui, Chenming Hu, and Ping K. Ko. "A robust and physical BSIM3 non-quasi-static transient and AC small-signal model for circuit simulation." Electron Devices, IEEE Transactions on 45, no. 4 (1998): 834-841.
[18] Smedes, T., and F. M. Klaassen. "An analytical model for the Non-Quasi-Static small-signal behaviour of submicron MOSFETs." Solid-state electronics 38, no. 1 (1995): 121-130.
[19] James, Ryan G., Korana Burke, and James P. Crutchfield. "Chaos forgets and remembers: Measuring information creation, destruction, and storage." Physics Letters A 378, no. 30 (2014): 2124-2127.
[20] Rosenstein, Michael T., James J. Collins, and Carlo J. De Luca. "A practical method for calculating largest Lyapunov exponents from small data sets." Physica D: Nonlinear Phenomena 65, no. 1 (1993): 117-134.
[21] Molnár, Kund, Gerhard Rappitsch, Zoltán Huszka, and Ehrenfried Seebacher. "MOS varactor modeling with a subcircuit utilizing the BSIM3v3 model." Electron Devices, IEEE Transactions on 49, no. 7 (2002): 1206-1211.