Ultrashort Terahertz Pulse Generation using 32nm CMOS Inverters

Sai Venkatesh Balasubramanian

Sree Sai Vidhya Mandhir, Mallasandra, Bengaluru-560109, Karnataka, India.
saivenkateshbalasubramanian@gmail.com

Abstract

An innovative design of millimeter wave electrical solitons using 32nm deep submicron technology is proposed and simulated at the layout (chip) level using Microwind software. The design is a CMOS differential sine oscillator followed by a single inverter acting as a sine-to-soliton converter which operates at 400GHz. The generation of robust self-starting solitons with simple circuitry forms the novelty of the present work.

Keywords: Electrical Solitons, Deep Submicron VLSI, Terahertz, CMOS

1. Introduction

In this era of ultra-high-speed telecommunications and computing reaching Terahertz frequencies[1], one of the significant issues the semiconductor industry constantly encounters is the problem of signal distortion[2]. This accounts for a certain amount of error in wired and wireless communications, as well as setting an upper limit to the speed achievable by computing devices. A simple mathematical signal-based analysis reveals that the fundamental source of such distortion is the presence of harmonics and the intermodulation distortion arising thereof[3]. The present work proposes an economically feasible, yet innovative solution to this problem, and the bottom-line is to use non-conventional hyperbolic secant based waveforms as carriers and as clock pulses. A special case of such waveforms, the solitons are known far and wide for their ability to propagate with almost zero distortion by striking a perfect balance between linear dispersion and nonlinear effects, and such waves have been put to enormous success in optical fiber communications[4].One of the primary issues that one encounters is the generation of electrical solitons at millimeter (mm) wave frequencies. The ability to produce such ultrafast solitons using a single CMOS inverter forms the novelty of the present work.

2. Methodology

The first step in the design of any CMOS deep submicron circuit is the selection of an appropriate technology[5]. In the present work, the technology files specified by the Predictive Technology Model (PTM)[6, 7] are used. The technology selected is a 32nm low-power high-k technology using metal Gate and strained Silicon[8]-[11]. The modelcard used is the default 32nm modelcard provided in the Microwind software, and is given in the Appendix. The layout consists of a CMOS differential sine oscillator, followed by a single CMOS inverter pair for the dark soliton generation composed of a PMOS-NMOS pair, followed by a similar CMOS inverter to invert the dark solitons, finally yielding bright solitons. This schematic is illustrated in Fig.(1). The PTM model is based on the standard BSIM4 MOS models[14]. For the simulation, Microwind[5], an open-source layout editor and simulator is chosen. The simulation timestep is set to 1fs. The layout of the CMOS inverter edited using Microwind is shown in Fig.(2). The 3D view including diffusion, polysilicon and metallization is shown in Fig.(3).

The generation of solitons in the proposed design can be attributed to the linear and nonlinear effects arising in the MOSFET. Of particular importance is the non-quasi static charge model of the MOS channel relevant at high frequencies, which states that the channel of a MOSFET can be modeled as a nonlinear transmission line. An illustration of the NQS model applied to the NMOSFET along with the drain, gate and source capacitances is shown in Fig.(4). Also, [15] gives the equivalent representation of the nonlinear transmission line by an Elmore resistance. This resistance is length dependant, which indicates the effect of wiring and transistor geometry in generation of solitons. The equivalent circuit of Fig.(4), with the Elmore resistance denoted by 'Re' is shown in Fig.(5). The dependance on the Elmore Resistance on the gate-source voltage V_{gs} is given as follows:

$$Re = \frac{L_{eff}}{10\mu_{eff}W_{eff}C_{ox}(V_{gs} - V_{th})} \tag{1}$$

where μ_{eff} is the effective carrier mobility, L_{eff} and W_{eff} denote the effective channel length and width of the NMOS transistor, C_{ox} denotes the oxide layer capacitance and V_{th} is the threshold voltage of the transistor.

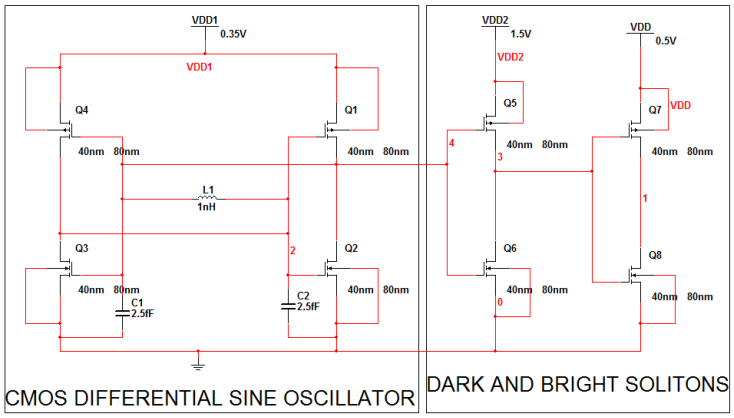

Figure 1: Schematic of the proposed CMOS Soliton Generator consisting of a single inverter

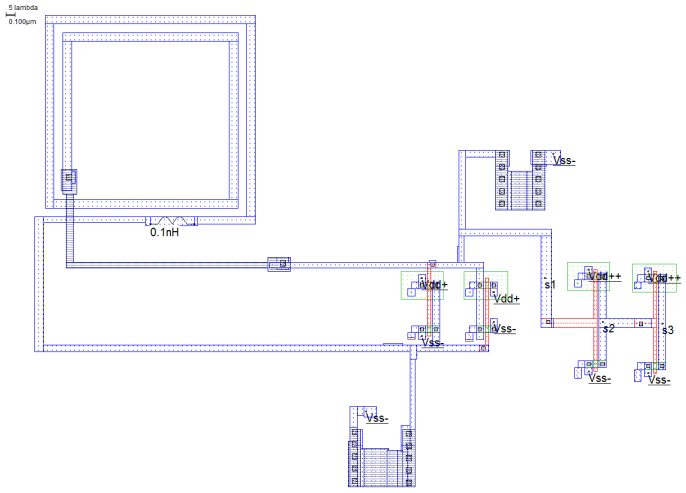

Figure 2: Layout of the CMOS Soliton Generator as obtained from Microwind

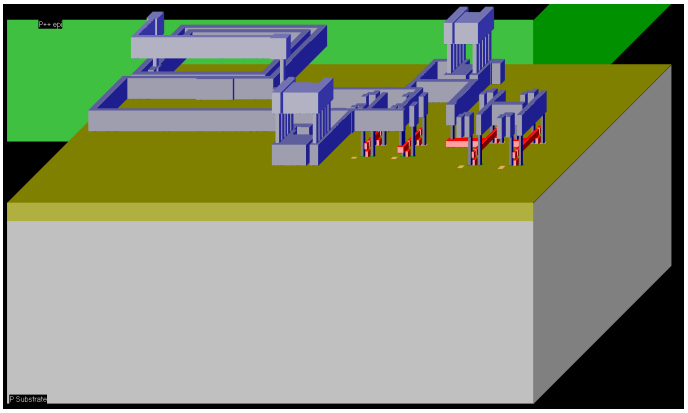

Figure 3: 3D View of the CMOS Soliton Generator as obtained from Microwind

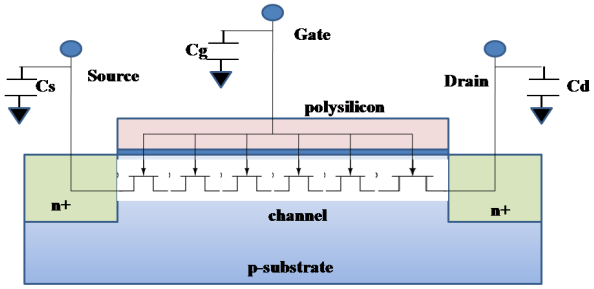

Figure 4: Non-quasi static representation of a NMOS channel

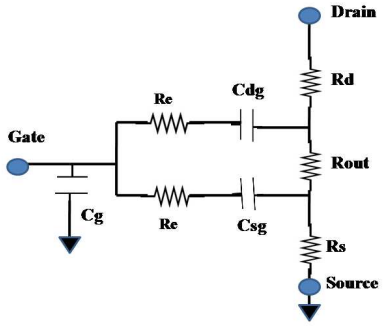

Figure 5: Equivalent circuit of non quasi static channel effect

3. Results and Discussions

The proposed layout is created using the Microwind software, and the extracted netlist is as shown in Fig.(6), indicating parasitic capacitances.

The waveform obtained at the end of the first inverter pair is a dark solitary wave train at a frequency of 400GHz, and this is shown in Fig.(7). One cycle of this waveform is taken and fitted with a negative hyperbolic secant squared pulse, with a Full-Width Half Maximum (FWHM) of 1ps, and a DC offset of 1V. This is shown in Fig.(8).

The transfer characteristics[12, 13] of a single CMOS inverter using 32nm technology is shown in Fig.(9).

The output obtained is a train of solitons, whose voltage waveform is shown in Fig.(10), and current waveform is shown in Fig.(11).

In order to ascertain the presence of solitons, one cycle of the output waveform was taken and fitted with hyperbolic secant squared waveform, with a Full-Width Half Maximum (FWHM) of 1ps. This is shown in Fig.(12).

The spectrum of the soliton output is shown in Fig.(13).

To understand the power dissipated in a single CMOS inverter, and to study its variations with respect to the voltage at its input, a parametric analysis is done. This is shown in Fig.(14).

4. Conclusion

A soliton generator at 400GHz was designed using 32nm strained silicon technology, and was implemented using Microwind software. The output waveforms were plotted, and the similarity to hyperbolic secant waveforms were obtained. Such solitary waves find immense applications in ultra-high speed computing and telecommunications. The sheer simplicity of the soliton generator is a huge economic advantage, and this forms the novelty of the present work. Future work includes a detailed BSIM4 based modeling of the inverter circuit and identifying the key physical phenomena underlying the soliton generation.

References

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* IC Technology: CMOS 32nm - 8 Metal
VDD 1 0 DC 0.35
V7_Vdd 7 0 DC 1.50V
V10_Vdd 10 0 DC 1.50V
* List of nodes
* "N2" corresponds to n°2
* "N3" corresponds to n°3
* "N4" corresponds to n°4
* "N5" corresponds to n°5
* "s3" corresponds to n°6
* "N8" corresponds to n°8
* "s2" corresponds to n°9
* "s1" corresponds to n°13
* MOS devices
MN1 0 9 6 0 N1  W= 0.08U L= 0.04U
MN2 0 13 9 0 N1  W= 0.08U L= 0.04U
MN3 13 15 0 0 N1  W= 0.08U L= 0.04U
MN4 0 13 15 0 N1  W= 0.08U L= 0.04U
MP1 7 9 6 5 P1  W= 0.08U L= 0.04U
MP2 10 13 9 4 P1  W= 0.08U L= 0.04U
MP3 13 15 1 3 P1  W= 0.08U L= 0.04U
MP4 1 13 15 2 P1  W= 0.08U L= 0.04U
C2 2 0  0.057fF
C3 3 0  0.058fF
C4 4 0  0.057fF
C5 5 0  0.058fF
C6 6 0  0.141fF
C7 7 0  0.068fF
C8 8 0  0.025fF
C9 9 0  0.205fF
C10 10 0  0.068fF
C11 11 0  0.023fF
C12 1 0  0.041fF
C13 13 0  2.567fF
C14 14 0  0.020fF
C15 15 0  1.170fF
C16 1 0  0.068fF
C17 17 0  0.018fF
* Extra RLC
Ladd1 15 13 0.1nH
* n-MOS BSIM4 :
* Standard
.MODEL N1 NMOS LEVEL=14
VTHO=0.18 U0=0.050 TOXE= 1.5E-9 LINT=0.000U
+K1 =0.450 K2=0.100 DVT0=2.300
+DVT1=0.540 LPE0=23.000e-9
ETA0=0.080
+NFACTOR=  1.6 U0=0.050
UA=3.000e-15
+WINT=0.020U LPE0=23.000e-9
+KT1=-0.060 UTE=-1.800 VOFF=0.010
+XJ=0.150U NDEP=170.000e15
PCLM=1.100
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p
* p-MOS BSIM4:
* Standard
.MODEL P1 PMOS LEVEL=14
VTHO=-0.18 U0=0.028 TOXE= 1.5E-9 LINT=0.000U
+K1 =0.450 K2=0.100 DVT0=2.300
+DVT1=0.540 LPE0=23.000e-9 ETA0=0.080
+NFACTOR=  1.6 U0=0.028 UA=3.000e-15
+WINT=0.020U LPE0=23.000e-9
+KT1=-0.060 UTE=-1.800 VOFF=0.010
+XJ=0.150U NDEP=170.000e15 PCLM=0.700
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p
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Figure 6: Extracted netlist as obtained from Microwind

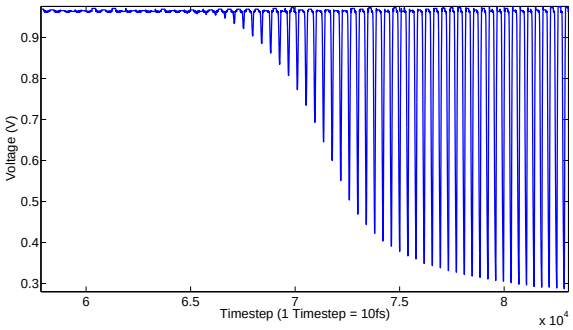

Figure 7: Voltage Output of the first CMOS inverter

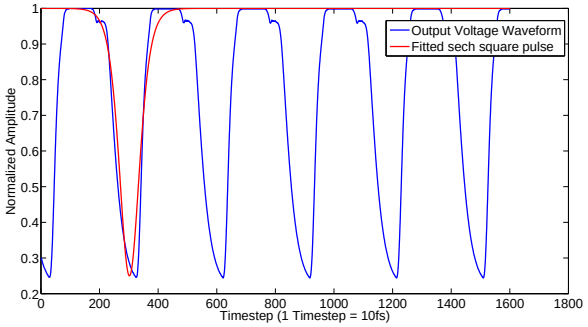

Figure 8: A section of the voltage output of the first CMOS inverter, fitted with a square of sech based pulse, with a FWHM of 1ps

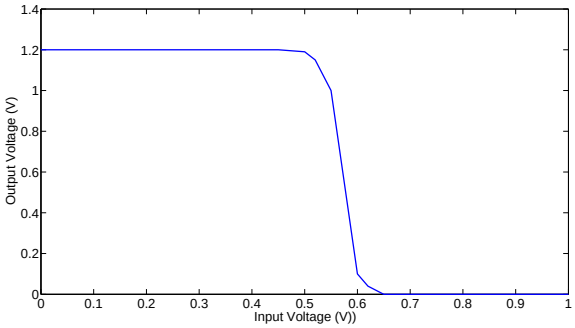

Figure 9: Transfer Characteristics of the inverter designed using Microwind

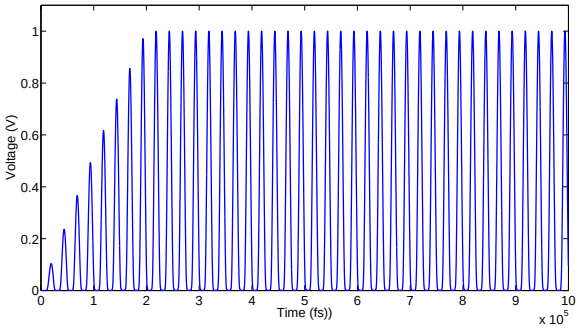

Figure 10: Final Output voltage waveform, showing bright solitons

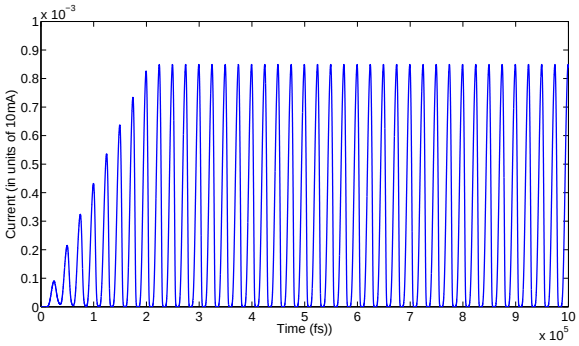

Figure 11: Final Output current Waveform, showing bright solitons

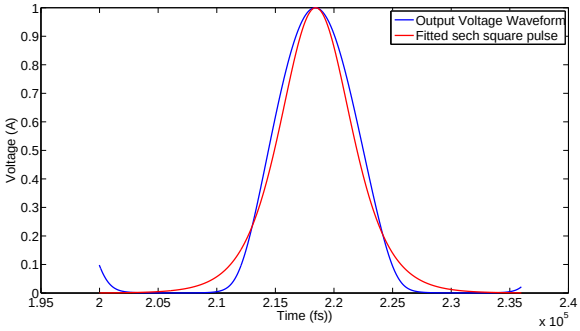

Figure 12: Solitary Wave fitted to square of sech, with a FWHM of 1ps. The output waveform is in blue, and the fit in red.

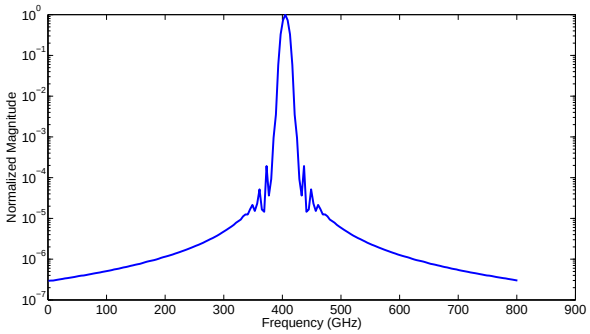

Figure 13: Spectrum of the output voltage Waveform

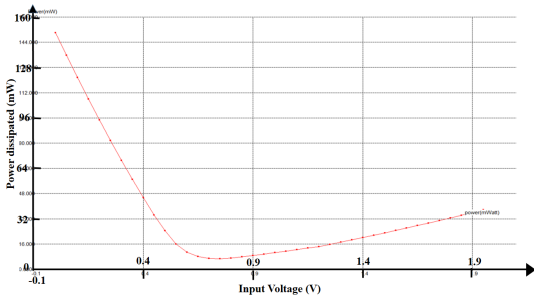

Figure 14: Power dissipated as a function of inverter input voltage, as obtained from Microwind

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