

Comparative Evaluation of SPWM Based 3 Level And 5 Level NPC Inverters with Reduced Switching Stress

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Abstract. The pulse sequence required for an NPC Inverter for 3 level and 5 level output is identified and is generated SPWM technique . The same pulses are generated using DSP F28335 kit and validated using a Digital Storage Oscilloscope. This project analyses multicarrier PWM methods for a single phase and three phase three level and five-level Neutral Point Clamped inverters. The advantages of a DSP based SPWM generation over conventional SPWM pulse generation are also studied. Using multilevel inverters, we get an output more sinusoidal, and hence having less harmonic content. But since the number of devices is more, the losses will be more compared to normal inverters, which can be reduced by employing space vector based PWM techniques or sinusoidal PWM based techniques. In this project, a multi-carrier based control technique is developed by the insertion of a zero voltage portion between every two half cycles.

Keywords: Neutral Point Clamped (NPC), Digital Signal Processor(DSP), Sine Pulse Width Modulation (SPWM)

1. Introduction

Among various multilevel topologies, the most accepted and well-known one is the 3 Level Neutral Point Clamped inverter [2], the power stage of which can be seen in Fig. 1. The only considerable disadvantage of this model, is that the semiconductor distribution losses distribution are imbalanced which causes poor thermal distribution. These losses are dependant over the PWM strategy employed in the model.

In a diode-clamped inverter, a single DC bus voltage is shared by a series of capacitors arranged as a string. An array of semiconductor switches and diodes make each leg of the three phase inverter capable of being switched to any of the available voltage levels. For example, in a 3 Level NPC Inverter, an array of 4 switches and 6 diodes make the leg of the NPC to be switched to $V_{dc}/2$, 0, $-V_{dc}/2$. The PWM strategies for this topology are well established. But still, to maintain the DC voltages of the capacitors balanced, some redundant switching regions are added [1]. A three-phase inverter has three legs, as depicted in Fig. 1. Every leg of the inverter has 4 semiconductor switches with anti-parallel diodes connected across each of them. There are also two clamping diodes in each arm. The switches of 1st leg are named S11 to S14 with their anti-parallel diodes Df11 to Df14. The switches S11 and S14 are called external switches and S12 and S13, internal. The switches S11 and S13 are triggered in a complementary manner. So are the switches S12 and S14.

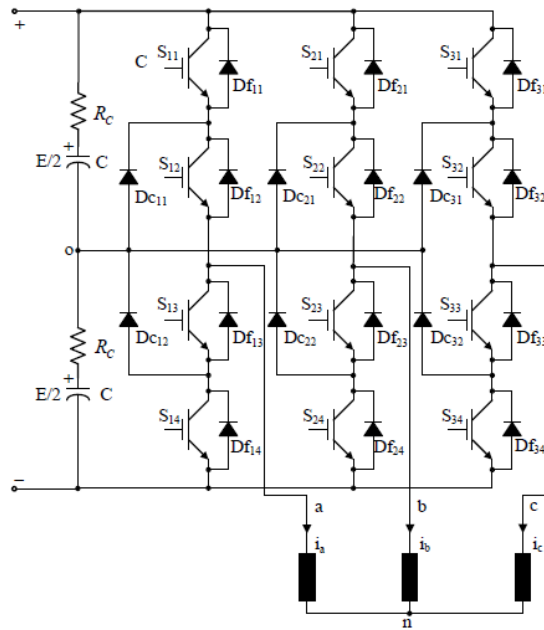


Figure 1 : 3 Phase 3 Level NPC Inverter

2. Methodology

2.1 Sinusoidal Modulation using Multiple Carrier Waves(SPWM)

In a sinusoidal PWM modulation a sinusoidal reference is compared with a triangular carrier. Here, in this project, we are implementing Multi-Carrier Based SPWM. According to the concept of Multi-Carrier Based SPWM, for an n level inverter, n-1 number of carrier signals is required. This methodology is done as illustrated in Figure 2.

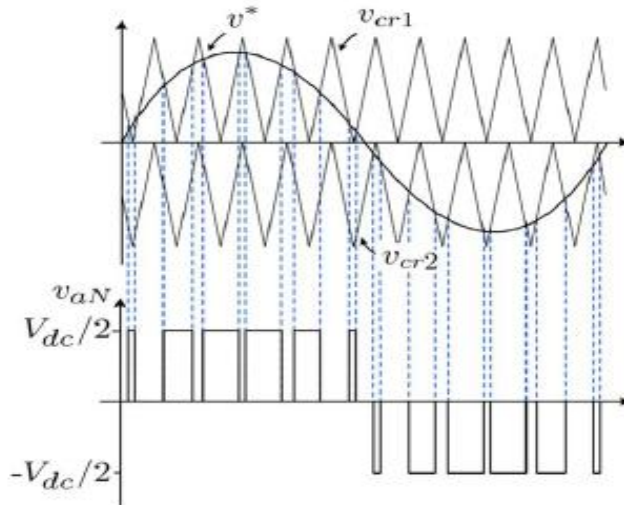


Figure 2 : Illustration of Multi-carrier SPWM

if $V^* > V_{cr1} \Rightarrow S_{11} = \text{ON } S_{12} = \text{ON } V_{an} = V_{dc}/2$
 if $V_{cr2} > V^* \Rightarrow S_{13} = \text{ON } S_{12} = \text{ON } V_{an} = 0$
 if $V^* > V_{cr2} \Rightarrow S_{13} = \text{ON } S_{14} = \text{ON } V_{an} = -V_{dc}/2$

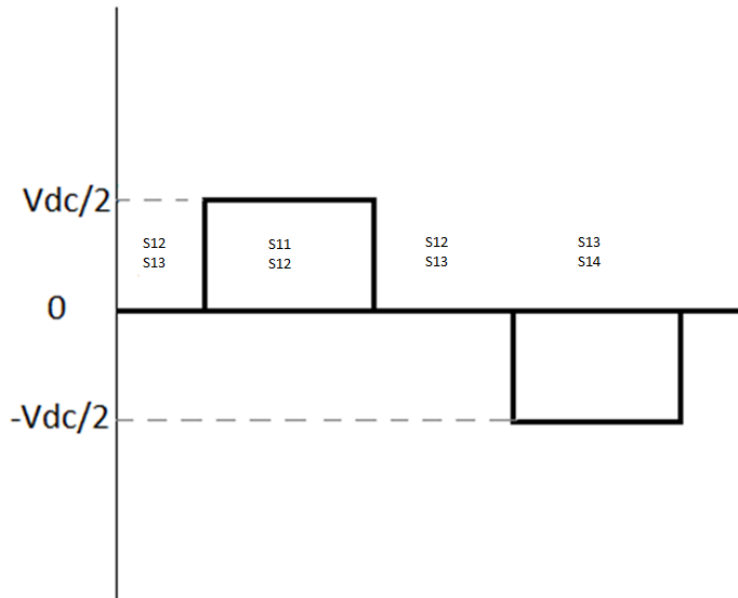


Figure 3: Switching sequence of one leg of a 3 Level NPC Inverter

2.2 DSP based SPWM pulse generation for 3 Level NPC Inverter

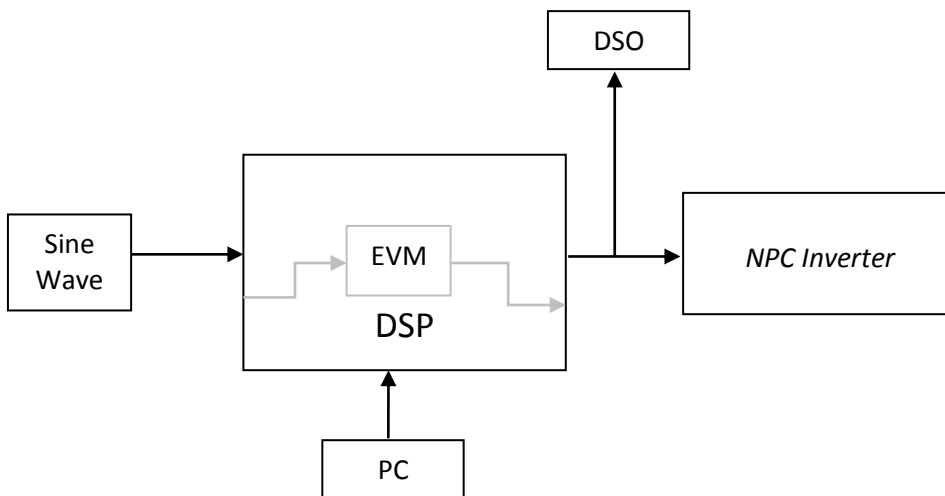


Figure 4: Block diagram of SPWM switching pulse generation using DSP

This model uses the ePWM (Enhanced Pulse Width Modulation) portions of the Event Manager Modules present in the DSP to generate PWM pulses. In the technique used in this project, sine wave, which is the reference signal, is

externally given as the compare value. The modulating signals, which are triangular pulses, are generated inside the Event Manager Block of the DSP by giving the suitable values. For providing pulses for the 4 switches, 2 ePWM modules each of the two Event Managers are used.

Each event manager can provide pulses for 6 switches, which together makes the DSP capable of controlling 12 switches.

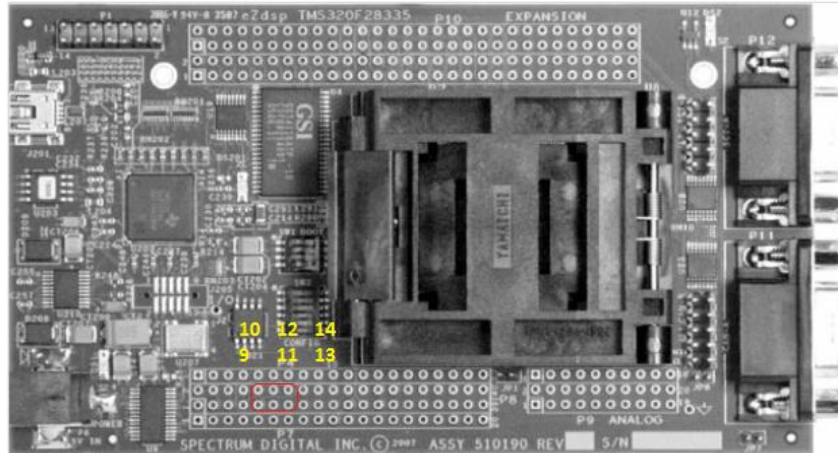


Figure 5: TMS320F28335 DSP kit with the ePWM output pins labelled

The outputs for 3 Level NPC Inverter is taken from the pins 9,10,11 and 12 which are ePWM1A, ePWM1B, ePWM2A, ePWM2B, ePWM3A and ePWM3B. For 5 Level NPC Inverter, pins 16 and 21 which are ePWM4A and ePWM4B are also used. Ground is obtained from the pins 19 and 20.

3. Level NPC Inverter

3.1 Simulated:

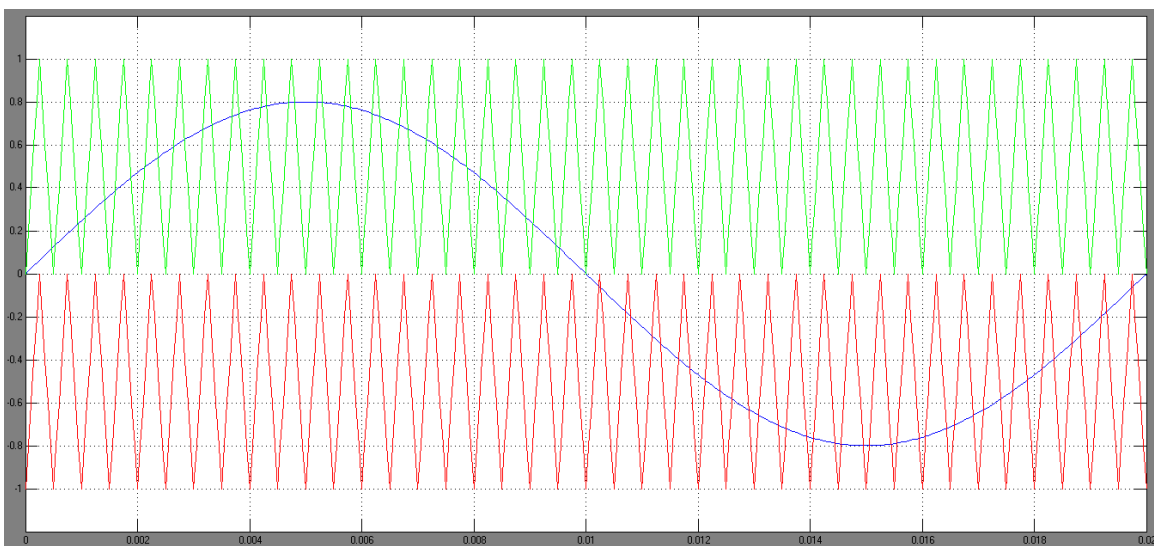


Figure 6: Multi-carrier comparison for 3 Level NPC Inverter in MATLAB-SIMULINK

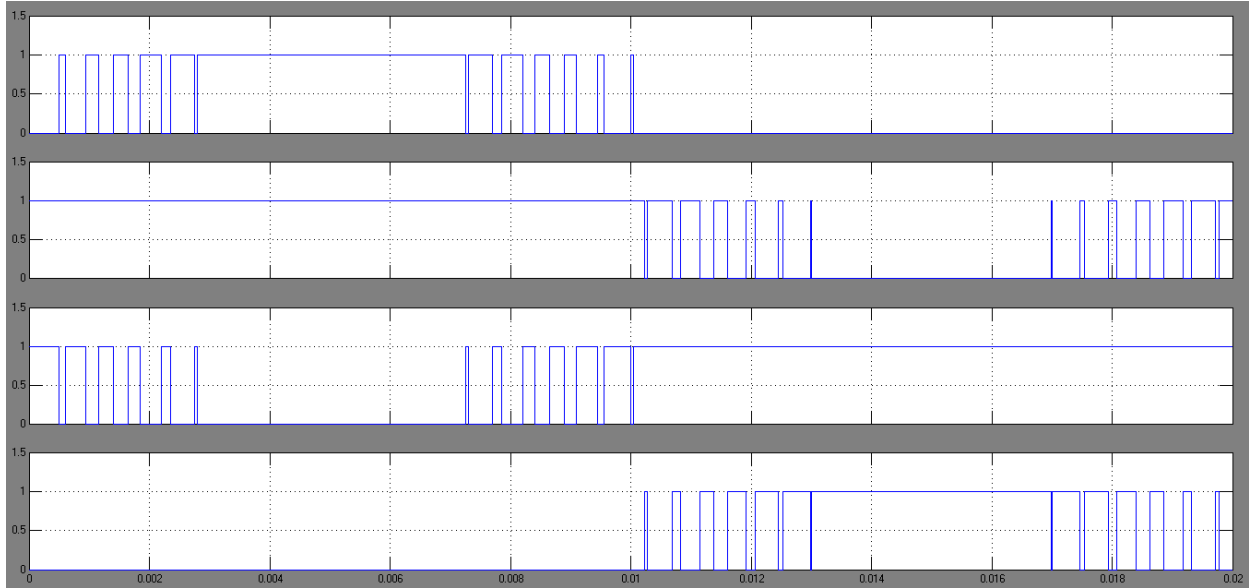


Figure 7: Switching pulses generated using SPWM for 3 Level NPC Inverter in MATLAB-SIMULINK

3.2 DSP-generated:

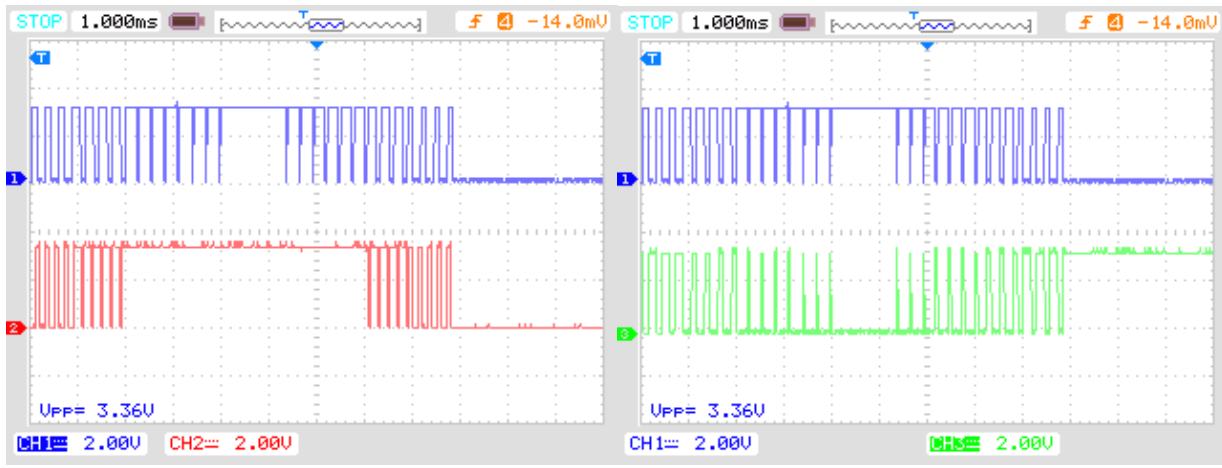


Figure 8: (a)Pulses for S11 and S12
(b)Pulses for S11 and S13

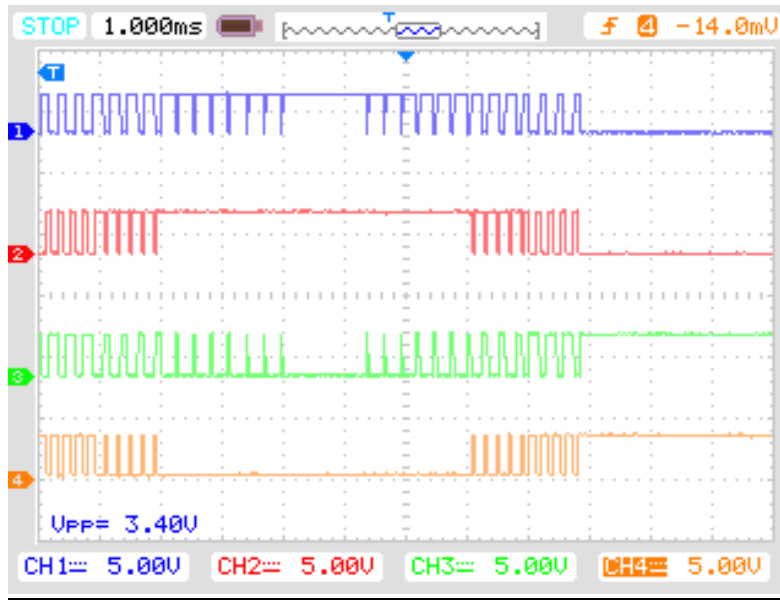


Figure 9: Switching pulses generated by DSP for S11, S12, S13 and S14

The pulses shown are in the order S11, S12, S13, S14. We can see from the sequence that S11 and S13 are complimentary to each other. i.e. one is the inverse of the other. This inverter can give output in 3 levels which are $V_{dc}/2$, 0 and $-V_{dc}/2$.

4. 5 Level NPC Inverter

4.1 Simulated:

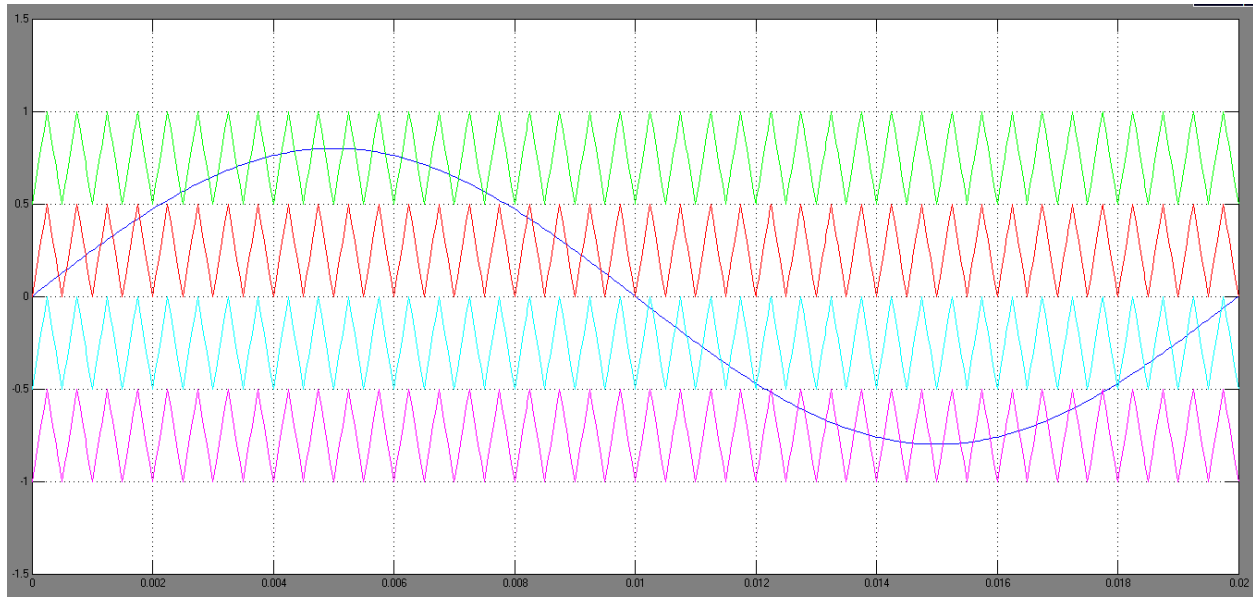


Figure 10: Multi-carrier comparison for 5 Level NPC Inverter in MATLAB-SIMULINK

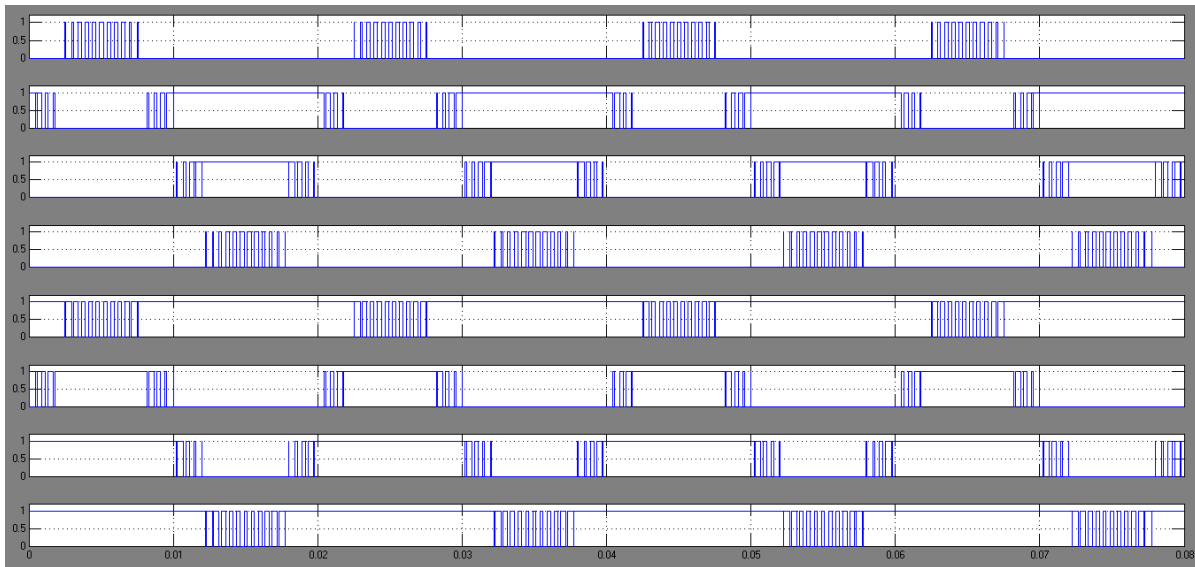


Figure 11: Switching pulses generated using SPWM for 5 Level NPC Inverter in MATLAB-SIMULINK

The pulses shown here are in the order S11, S12, S13, S14, S15, S16, S17, S18. We can see from the sequence that S11 and S15 are complimentary to each other. i.e. one is the inverse of the other. This inverter can give output in 5 levels which are $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$.

4.2 DSP-generated:

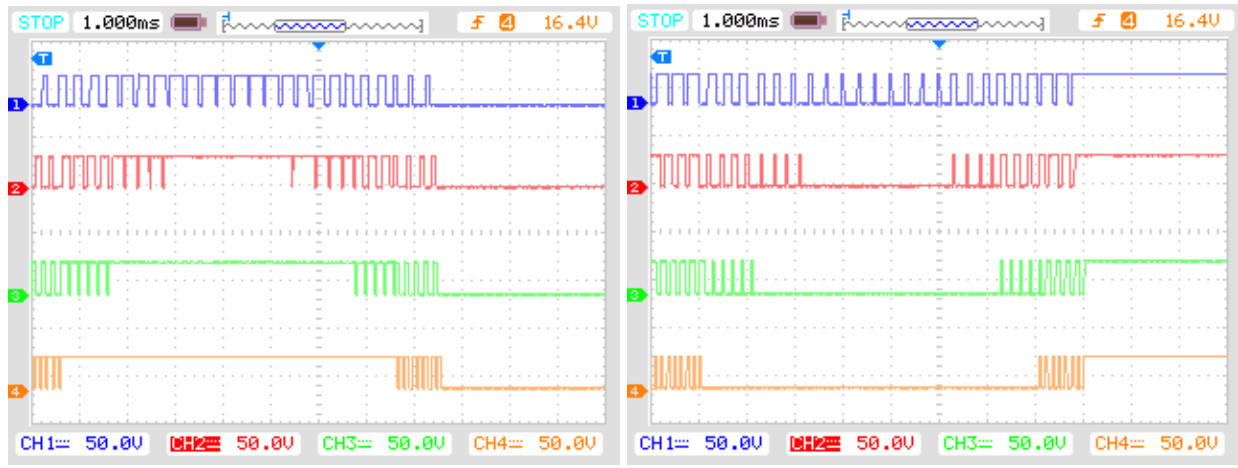


Figure 12: DSP-generated switching pulses for
 (a) 4 upper switches
 (b) 4 lower switches
 of a 5 Level NPC Inverter

5. Results and Discussion

5.1 Simulated:

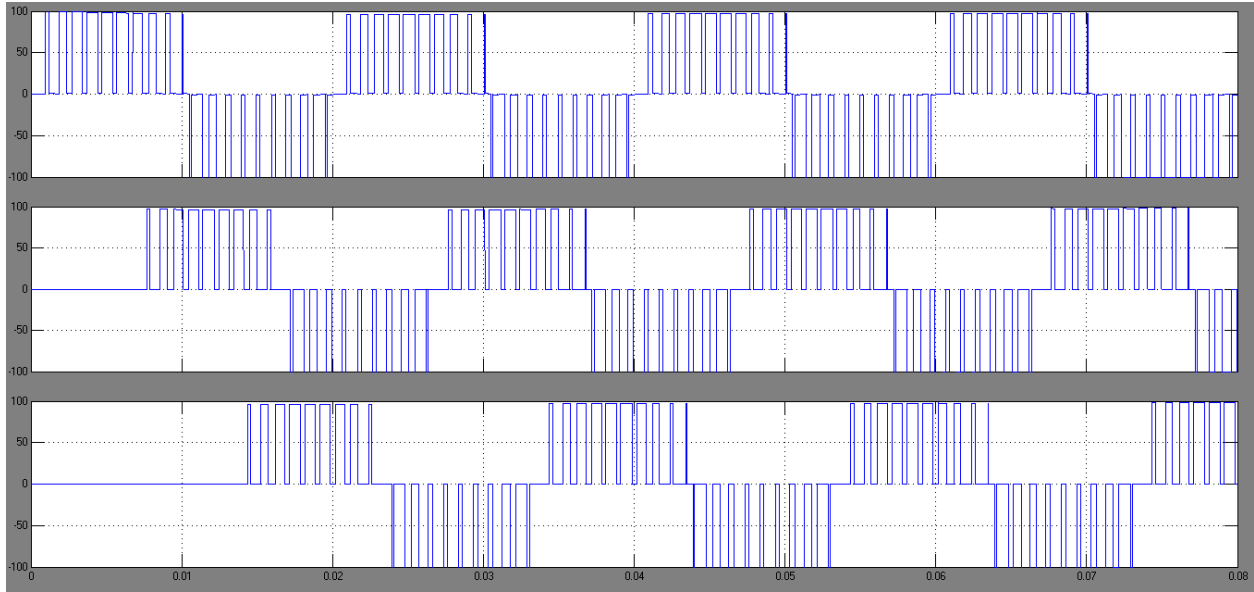


Figure 13 : Output Phase Voltages of the 3 level NPC

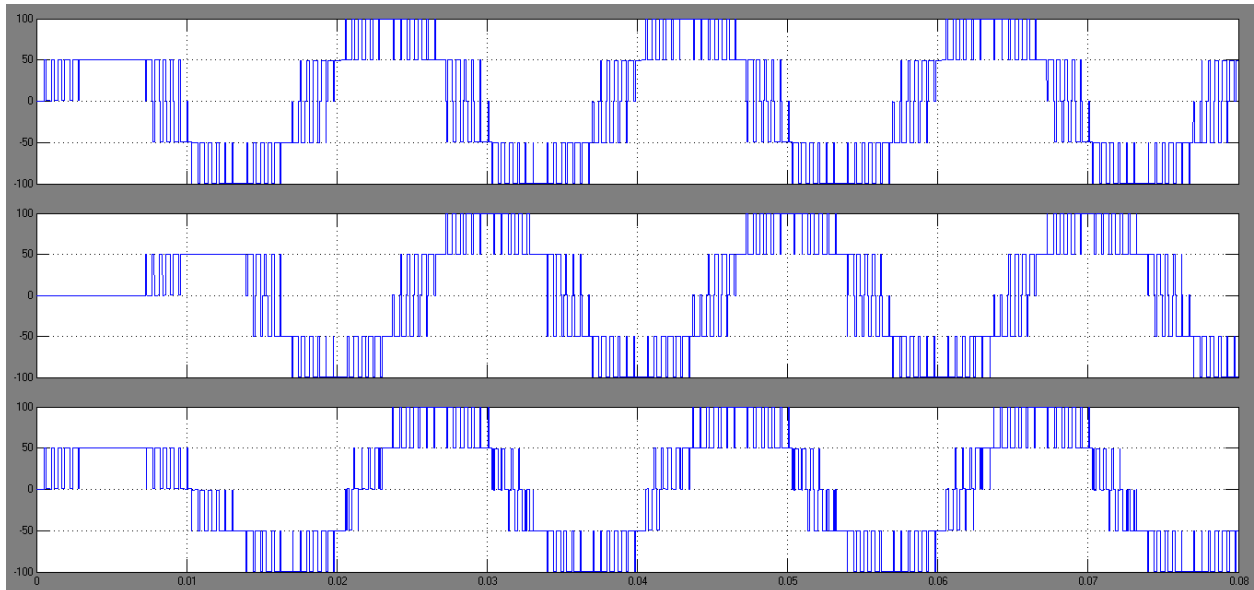


Figure 14: Output Line Voltage of the 3 level NPC

It can be noted from the output waveforms that there are 3 levels or steps which makes the output resemble a sine wave and hence reducing the harmonics. The FFT analysis of this waveform is given below.

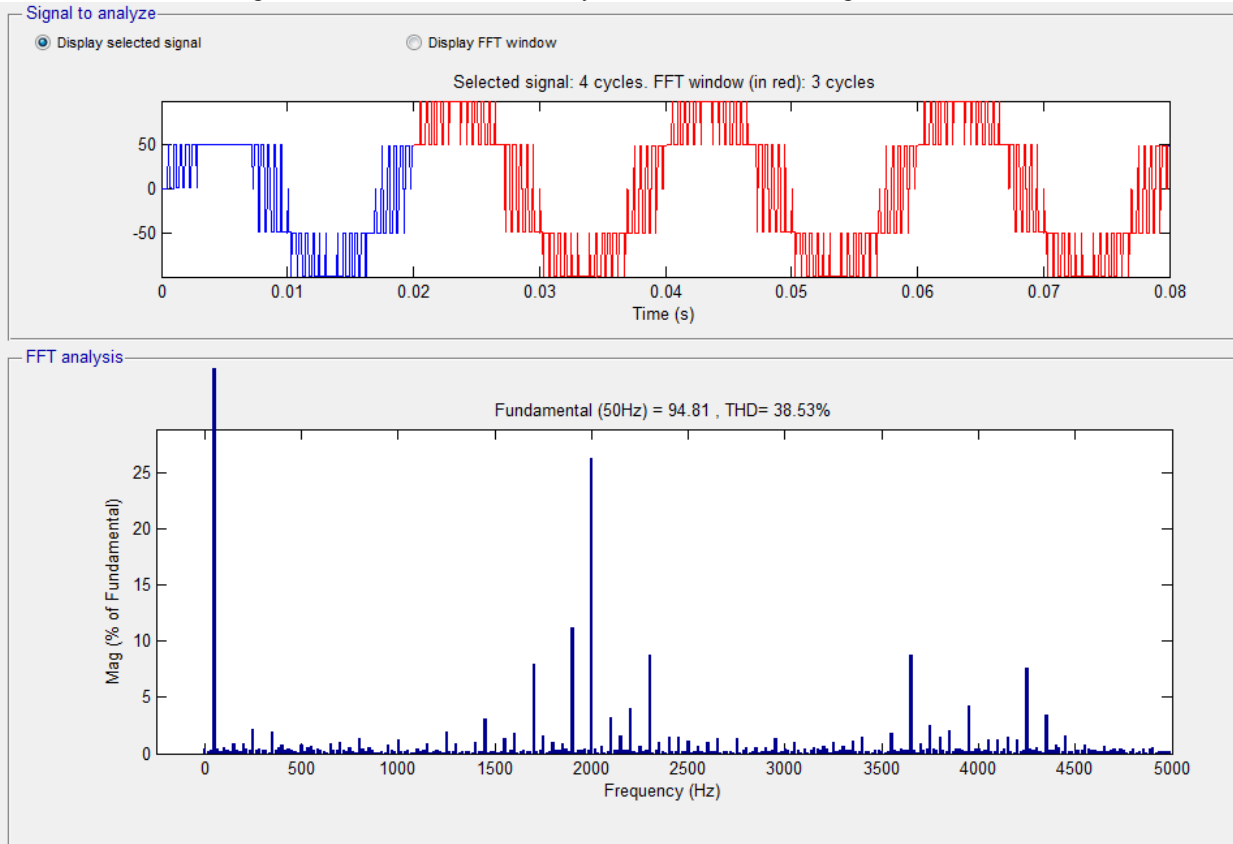


Figure 15: FFT Analysis of the Line Voltage Output of the 3 level NPC inverter

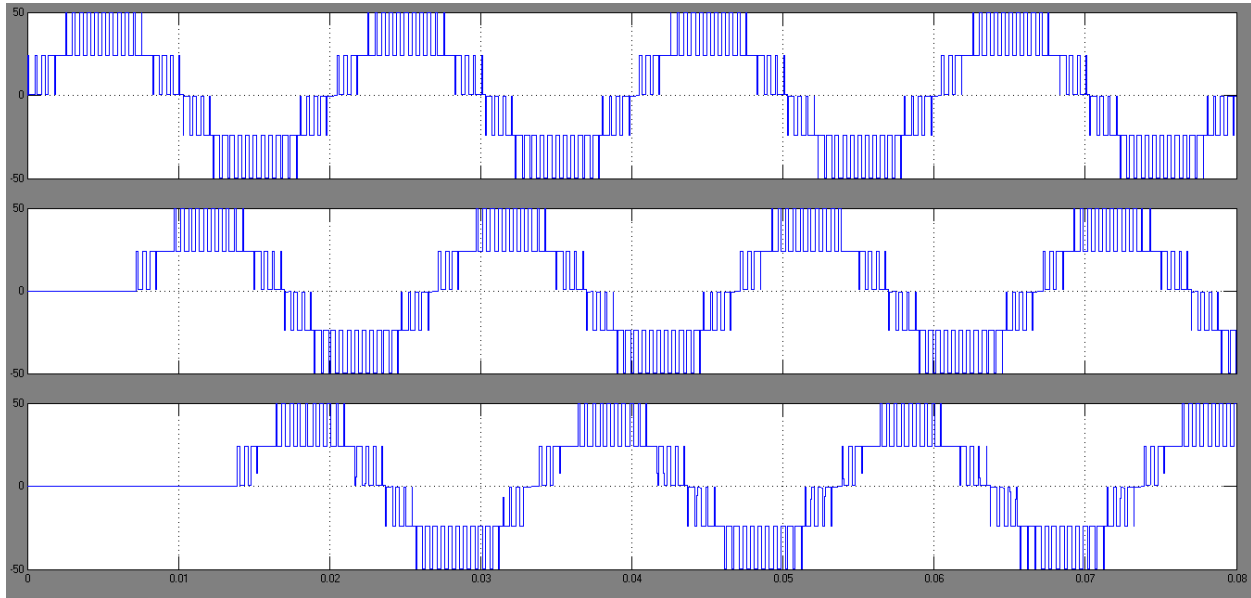


Figure 16 : Output Phase Voltages of the 5 level NPC

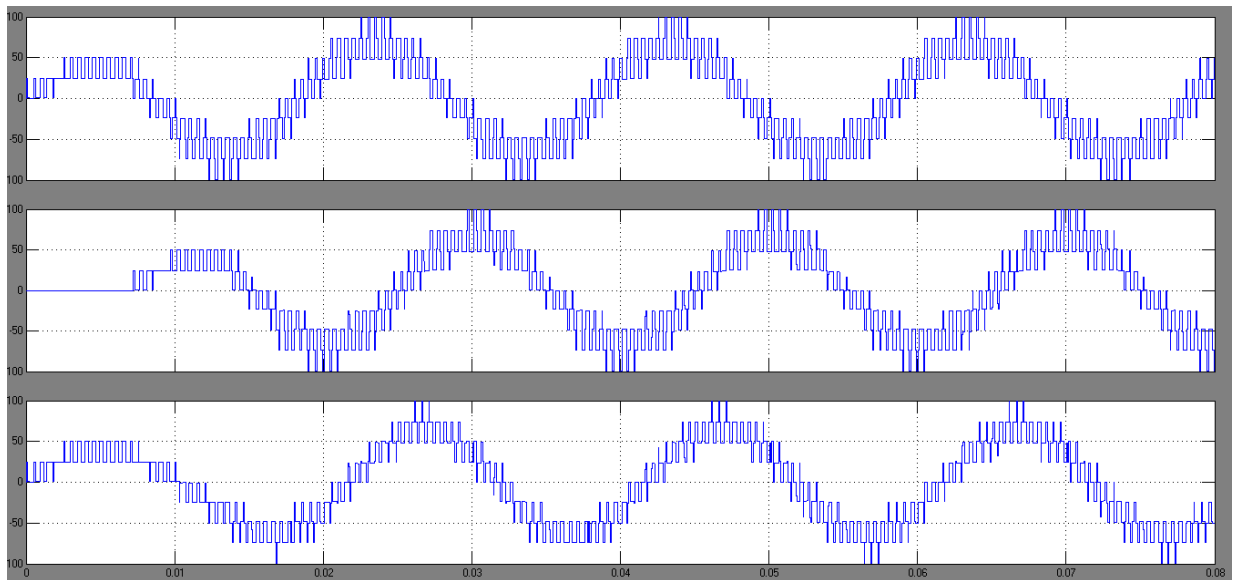


Figure 17 : Output Line Voltages of the 5 level NPC

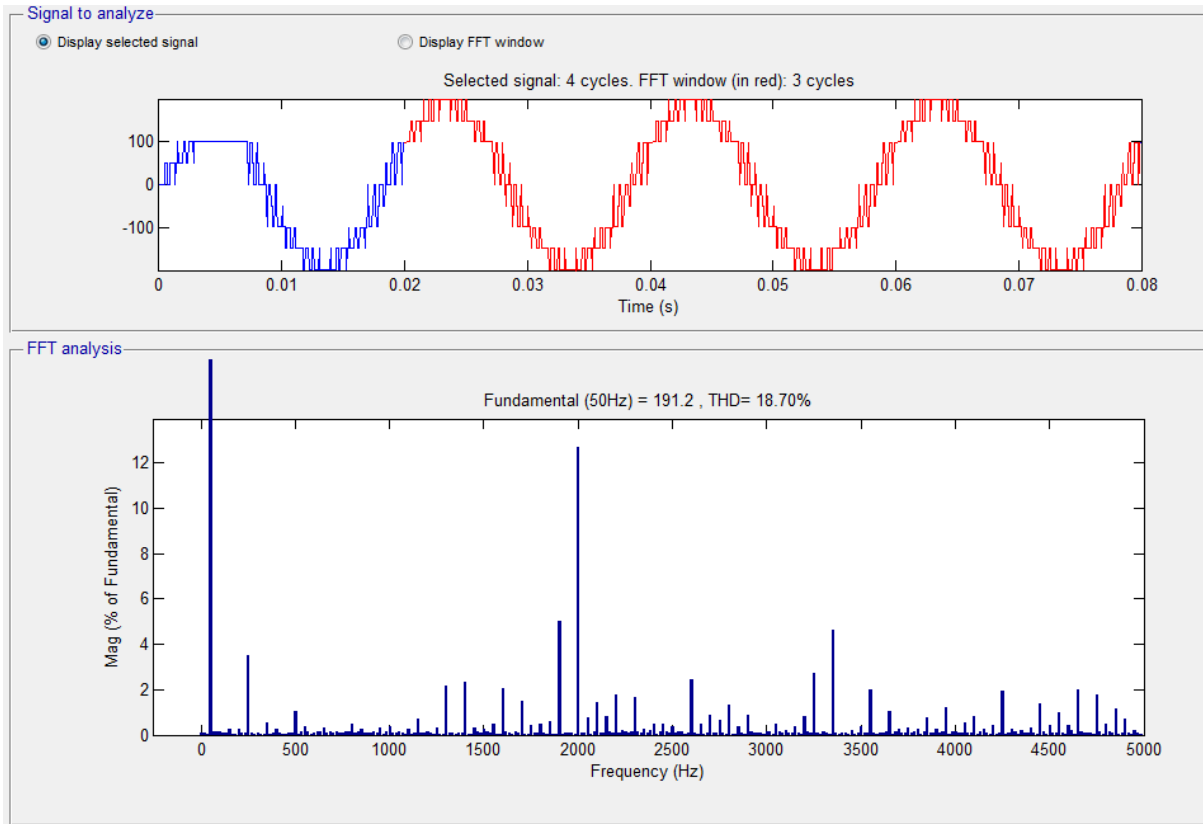


Figure 18: FFT Analysis of the Line Voltage Output of the 5 level NPC inverter

5.2 Comparison:

Parameter	3 Level NPC Inverter	5 Level NPC Inverter
No. of switches in a leg	4	8
THD	38.53%	18.70%
Fundamental	94.81%	191.2%
Voltage Levels available	3	5
Maximum voltage stress on 1 switch	$V_{dc}/2 = 100$	$V_{dc}/4 = 50$

Table 1 : Comparison of 3 Level and 5 Level NPC Inverters

6. Conclusion

3 Level and 5 Level NPC Inverters are simulated and compared. It was inferred that as the number of levels in an Inverter increase, the harmonic distortion as well as voltage stress over each switch reduces considerably. The switching pulses required for 3 Level and 5 Level NPC Inverters are generated using DSP TMS320F28335 kit and validated using a Digital Signal Oscilloscope. This work can be extended in the future by avoiding SPWM for the OFF region of the switches alone and thus reduce the switching losses to a very great extend.

7. References

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