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# A New Approach for Current-Mode SRD Filters

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**Abstract.** In this paper a new geometric-mean circuit for current-mode square-root domain filters (SRD) is presented. The geometric-mean circuit employs MOSFET transistors that are operating in both strong inverted saturation and triode regions and works in low supply voltage. Simulation results by HSPICE confirm the validity of the proposed design technique.

**Keywords:** Geometric mean, companding filter, current-mode.

## 1 Introduction

Companding (compressing and expanding) filters as an attractive technique in analog circuit designs have drawn the attention of many researchers. The main advantage of these filters is their large dynamic range in low voltage, caused by voltage swing reduction at internal nodes [1]. In the first attempt companding systems employed the exponential I-V characteristic of bipolar transistors that led to the log-domain structures [2, 3]. Developments in CMOS circuits and also similarity in I-V characteristics, caused the bipolar transistors were substituted by CMOS transistors that are operating in weak inversion region [4]. However, the effects of limited speed and transistor mismatches restricted their applications. Afterwards, companding system employed MOS transistors in saturation region based on voltage translinear principle and class-AB linear tranconductors that led to square-root domain (SRD) structure [5-13]. The main drawback of these circuits is that for correct operation, all MOS transistors of the circuit should work in saturation region. If, in some cases, the transistors are forced to enter triode region, it will invalidate the MOS translinear or tranconductance operation, which lead to more nonlinearity. In this work to overcome the above problem a new approach for geometric-mean circuit as the basic unit of SRD filters is presented, in which MOS transistors operate in both saturation and triode region and the circuit can work in low supply voltage.

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This paper is organized as follows: In section 2, the basic principle of current-mode SRD filters operation is presented. In section 3 circuit design of proposed geometric mean is presented. In section 4 and 5 simulation results and conclusion is presented, respectively.

## 2 Principle operation of SRD filters

A current-mode first-order low pass filter with output current $I_{out}$ and input current $I_{in}$ in time domain will be expressed by [1].

$$(1)\ \tau \frac{dI_{out}}{dt} + I_{out} = AI_{in}$$

in which, $A$ is the DC gain, $\tau = \frac{1}{\omega_C}$ is the time constant of filter and $\omega_C$ is cutoff frequency of the filter.
Fig. 1 shows the basic principle of the SRD filter. Employing I-V relation of transistor MF gives:

$$(2)\ I_{out} = \frac{\beta}{2}\left(V_{cap} - V_{th}\right)^2$$

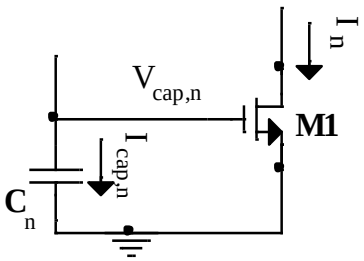



**Fig. 1:** principle of the SRD filter

It can be shown [1], after a little manipulation by substituting (2) into (1), it gives:

$$(3)\ I_{cap} = I_{in}\sqrt{\frac{I_{tune2}}{I_{out}}} - I_{out}\sqrt{\frac{I_{tune1}}{I_{out}}}$$

in which , tuning current $I_{tune1}$ and $I_{tune2}$ are obtained by [1]:

$$(4)\ I_{tune1} = \frac{\left(C\omega_C\right)^2}{2\beta} \quad , \quad I_{tune2} = \frac{\left(AC\omega_C\right)^2}{2\beta}$$

Fig. 2 shows block diagram of the SRD first-order LPF based on (3).

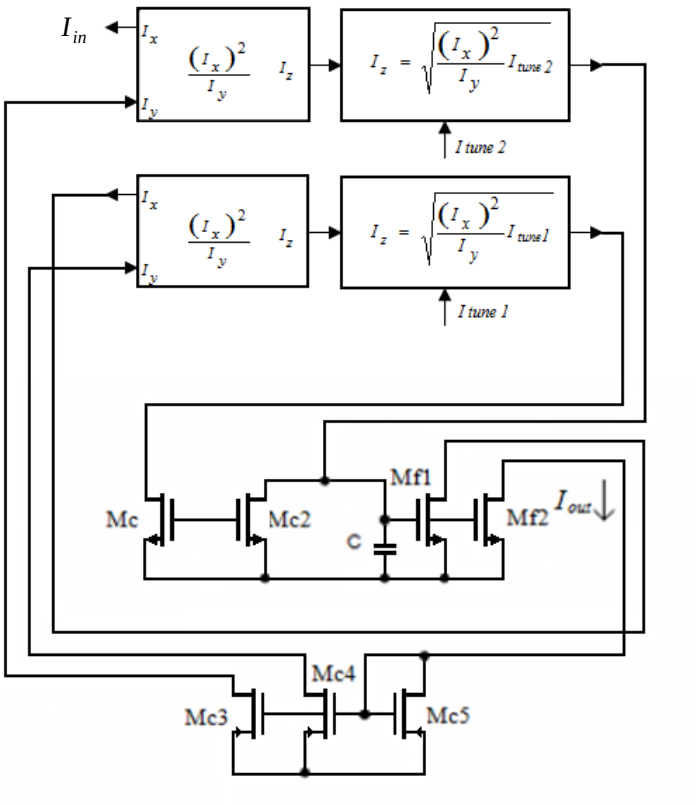



**Fig.2:** Block diagram of the SRD first-order LPF

## 3 Circuit Design

Fig. 3 shows the proposed geometric-mean circuit that contains of two current mirrors by transistors M1, M2, M7 and M5, M6, M12, respectively, output current mirror (transistors M13-M16) and auxiliary transistors (M3, M4, M8-11). Input currents are $I_x$, $I_y$ and output current is $I_{out}$ of the geometric-mean circuit. In a simple analysis, it is assumed that the bulk effect and channel-length modulation are not be considered and those effects will be apparent in the simulation results. In this circuit it is considered that transconductance factor of M1, M2, M5 and M6 are identical. In this case the current drain of MOS transistors that are operating in triode region is:

$$I_D = \beta\left[(V_{GS} - V_{DS})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad (5)$$

and for saturation region it will be:

$$I_D = \frac{\beta}{2}(V_{GS} - V_{th})^2 \Rightarrow V_{GS} = \sqrt{\frac{2I_D}{\beta}} - V_{th} \quad (6)$$

It can be shown when input current $I_x$ is higher than other input current $I_y$ ($I_x > I_y$), transistor M2 and M3 operates in triode region and transistor M4 and M5 operates in saturation region and vice versa .

Assuming that M8 and M11 are identical and having the aspect ratio of $(N_1)^2$ times more than the aspect ratio of the M1, M2, M5 and M6, then transconductance factor of the M8 and M11 will be [13]:

$$(7)\ \beta_8 = \beta_{11} = (N_1)^2\beta$$

With this assumption and by considering Fig. 4, and using (5) and (6), the drain-source voltage of transistor M2 can be written as follows:

$$V_{DS2} = V_{GS11} - V_{GS10} == \sqrt{\frac{2}{\beta}}\left(\sqrt{I_y} - \frac{\sqrt{I_{M2}}}{N_1}\right) \quad (8)$$

According to prior assumption ($I_x > I_y$), M2 operate in triode region, so from (5), (6) and by applying (8), it can be shown that the drain current of M2, by assumption that $N_1^2$ is much more than one, will be:

$$I_{M2} \cong (2\sqrt{I_x I_y} - I_y - \frac{2}{N_1}\sqrt{I_{M2}}(\sqrt{I_x} - \sqrt{I_y})) \quad (9)$$

that reported in [13]. In this work, aiming to better performance of the output current of the geometric mean circuit and thus elimination the second and third terms of right hand side of (9), it is assumed that transcodutance factors of M3 and M4 is:

$$(10)\ \beta_3 = \beta_4 = \frac{\beta}{2}$$

and

$$(11)\ \beta_9 = \beta_9 = \frac{N_2^2\beta}{2}$$

which lead to better approximation rather than existed in proposal [13].
Similar to (8) and using (10) and (11), the drain-source voltage of transistor M3 will be:

$$(12)\ V_{DS3} = V_{GS6} - V_{GS10} = \sqrt{\frac{2}{\beta}}\left(\sqrt{I_y} - \frac{\sqrt{I_{M2}}}{N_1}\right)$$

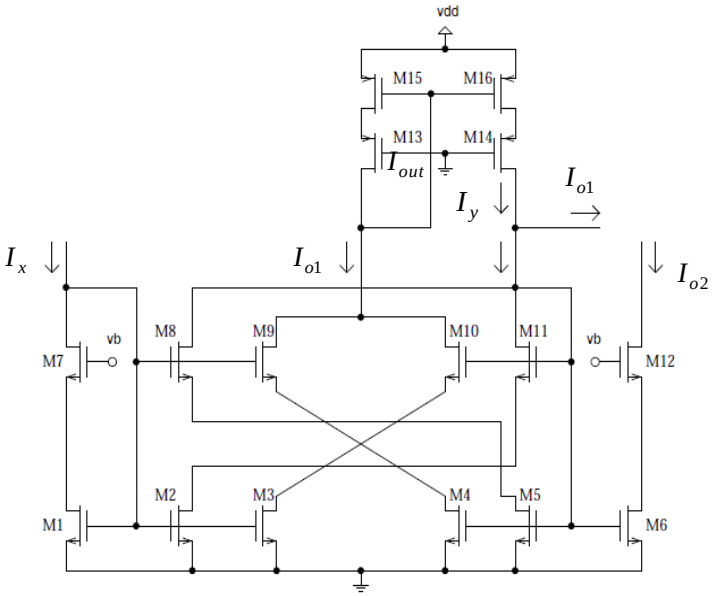



**Fig.3** : proposed geometric mean circuit

And, by assumption that $N_2^2$ is much more than one, the current drain of M3 approximately will be:

$$I_{M3} \cong (\sqrt{I_x I_y} - \frac{I_y}{2} - \frac{1}{N_2}\sqrt{I_{M3}}(\sqrt{I_y} - \sqrt{I_x}) \qquad (13)$$

In Fig. 3, the output current $I_{o1}$ is summation of the drain current of transistors M9 and M10 (or equivalently summation of the drain current of transistors M3 and M4). So, by applying KCL in node A and using (9):

$$(14) = \sqrt{I_x I_y} - \frac{2}{2N_2}\sqrt{I_{M3}}\left(\sqrt{I_y} - \sqrt{I_x}\right) \; I_{o1} = I_{M3} + I_{M4} = I_{M3} + \frac{I_y}{2}$$

Also the output current $I_{o2}$ is summation both drain current of M8 and M11. Similarly, by applying KCL in node B and using this assumption that $\beta_5 = \beta_6$, the output current $I_{o2}$ will be expressed as: $I_{o2} = I_{M2} + I_y$, and using (9), the current $I_{o2}$ will be:

$$(15) \; I_{o2} = 2\sqrt{I_x I_y} - \frac{2}{N_1}\sqrt{I_{M2}}\left(\sqrt{I_y} - \sqrt{I_x}\right)$$

Now by applying KCL in node X of Fig. 3, the output current will be obtained by:

$$I_{out} = I_{o1} - I_{o2} = \sqrt{I_x I_y} - \frac{2}{N_1}\sqrt{I_{M2}}\left(\sqrt{I_y} - \sqrt{I_x}\right) + \frac{2}{2N_2}\sqrt{I_{M3}}\left(\sqrt{I_y} - \sqrt{I_x}\right) \quad (16)$$

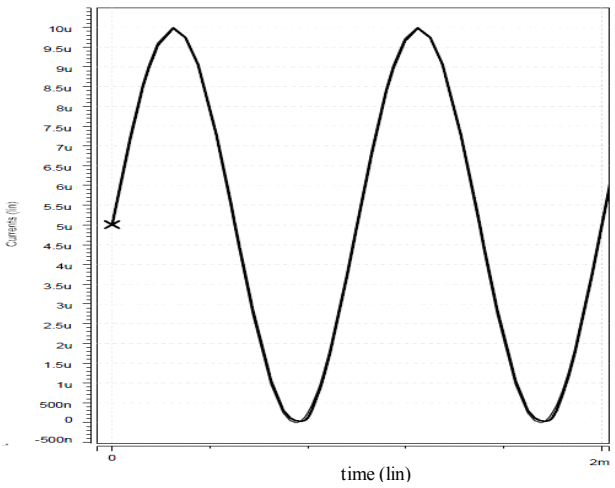
and using (9), it results: $I_{M5} = \frac{I_{M2}}{2}$ , so it can be seen if in (16) it is considered that $N_2 = \frac{N_1}{2\sqrt{2}}$, then the output current $I_{out}$ simplified to:

$$I_{out} = \sqrt{I_x I_y} \quad (17)$$

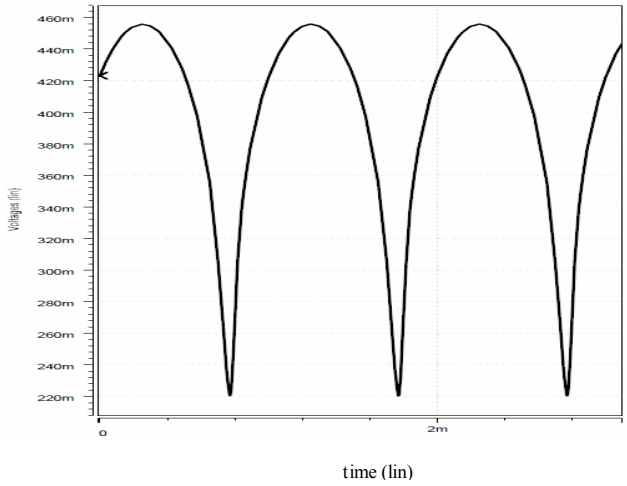
From (17), it can be seen that the proposed circuit acts as a geometric-mean. It is evident that squarer/divider is obtained by exchanging the output current $I_{out}$ with one of input $I_y$ of geometric mean circuit.

## 4 Simulation Results

By employing block diagram of Fig. 2 and using circuit diagram of Fig. 3 a current mode first order low pass filter is designed and simulated by HSPICE. $V_{dd}$=1V and an external capacitor C=50pF were employed. Transient analysis were carried out by using $I_{tune1}$=$I_{tune2}$=15uA as shown in Fig. 4. Fig. 4 shows time response of the filter for sinusoidal input current with 5uA amplitude, 5uA bias current and with 1 kHz frequency. The frequency response of the filter is tunable. Fig. 5 shows frequency response simulation, with varying tuning current in range of 6uA to 10uA (from left to right). Fig. 6 shows the nonlinear behavior of the output current by using total harmonic distortion with a 4096 point Fast Fourier (FFT). The worst-case THD of the output the current is less than -40db for the input amplitudes from 10uA to 45uA.




(a)




(b)

**Fig. 4:** Time Response of the filter a: input and output filter b:capacitor voltage

5uA bias current and with 1 kHz frequency. The frequency response of the filter is tunable. Fig. 5 shows frequency response simulation, with varying tuning current in range of 6uA to 10uA (from left to right). Fig. 6 shows the nonlinear behavior of the output current by using total harmonic distortion with a 4096 point Fast Fourier (FFT). The worst-case THD of the output the current is less than -40db for the input amplitudes from 10uA to 45uA.

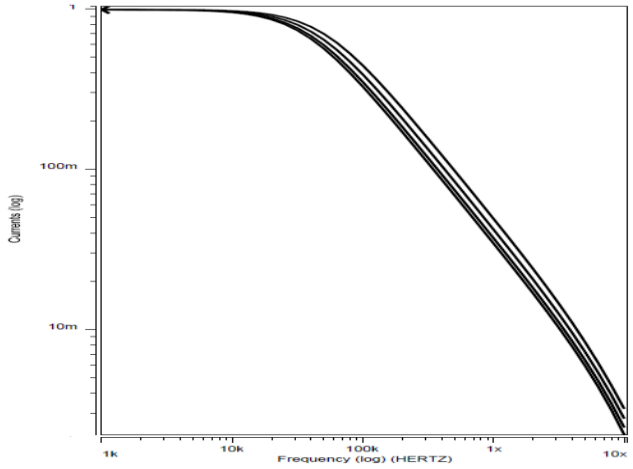



**Fig. 5:** Frequency response of the filter

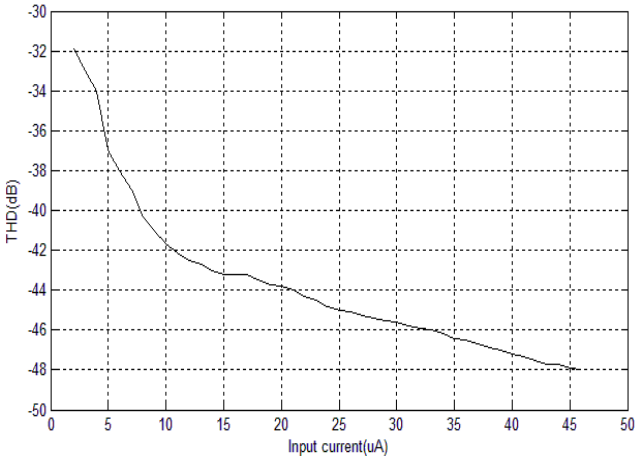



**Fig. 6:** Nonlinearity performance of the filter

## Conclusion

In this paper a new current-mode geometric-mean that uses MOS transistors that are operating in both saturation and triode region is presented. Simulation results of the filter show that the proposed technique is applicable to design of filters with low voltage requirement. The circuit is employed for designing of a first order SRD filter.

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