Analog Realization of a Fractional-Order Element on 0.35μm CMOS Technology

Alexander C. Abad, Emmanuel A. Gonzalez, Roderick Y. Yap, and L'ubomír Dorčák

***Abstract*—In this short note, we present the analog realization of a fractional-order differentiator of order $\alpha = 1/2$ in 0.35 μm CMOS technology.**

I. Overview

This short note presents the use of 0.35 μm analog CMOS technology in the development of a fractional-order differentiator of order $\alpha = 1/2$ which is also known as a *semi-differentiator*. A semi-differentiator has a continuous-time transfer function of

$$G(s) = s^{\alpha}, \tag{1}$$

where α is constant at 0.5. In general, a transfer function of such form where α is an arbitrary real number can be considered as a *fractional-order system*, having various applications sciences and engineering [1], [2]. A semi-differentiator will have a magnitude slope of 10dB/dec and a phase angle of 45 degrees all throughout the entire frequency range.

A semi-differentiator can be realized using operational amplifier (op-amp) circuits, i.e. series combination of an inverting amplifier and an analog inverter of unity gain. The impedance of the op-amp circuit becomes

$$G(s) = \frac{V_O(s)}{V_i(s)} = \frac{Z_F(s)}{Z_A(s)} = \frac{R}{\frac{1}{Cs^{\alpha}}} = RCs^{\alpha}. \tag{2}$$

If it is assumed that $RC = 1$ and that $\alpha = 1/2$, then (2) becomes equal with (1). To achieve this result, it is important to make the arm element dictated by $Z_A(s)$ have a transfer function of the order $\alpha = 1/2$, which could be achieved by using RC ladders. Such concept has been implemented in [3], [4] with its latest method coming from [5].

II. Solid-State Electronic Circuit Realization

To achieve a semi-differentiator op-amp circuit, the following resistance and capacitance values have been obtained and simulated using LTSpiceIV as shown in Fig. 1. The computation details in the determination of these values will be published later. The frequency response of the circuit in Fig. 2

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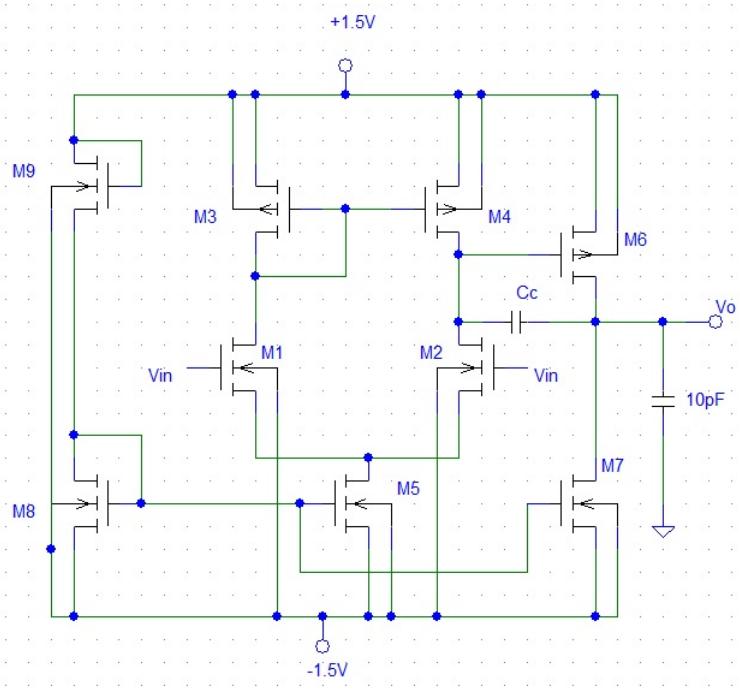

Figure 3. Selected microelectronic op-amp topology based on [6].

III. CMOS Analog Realization

Fig. 3. presents the analog microelectronic op-amp circuit chosen in the realization of a semi-differentiator which has been borrowed from [6]. The objective of the design is to compute the sizes of all transistors of the op-amp.

The sizes of transistors computed based on [6] are shown in Table I. The size of the transistor is the width-to-length ratio of the transistors. In this design, all transistors have the length of 1μm. Thus, sizes will be the equivalent transistor width. There is a slight deviation on the size of M6 to correct the dc offset of the op-amp during simulation. The size of M9 was rounded up to 1.0 for easy layout without significant effects on the op-amp's bias.

Table II presents the resulting parameters of the designed op-amp.

Fig. 4 presents the layout of the inverting amplifier with a gain of 20. The layout covers an area of 90 $\mu m \times$ 113.5 μm. Fig. 5, on the other hand, presents the top-level layout of the entire semi-differentiator which measures 7.2415 mm $\times$ 3.7545 mm, in which most of the area is covered by NMOS

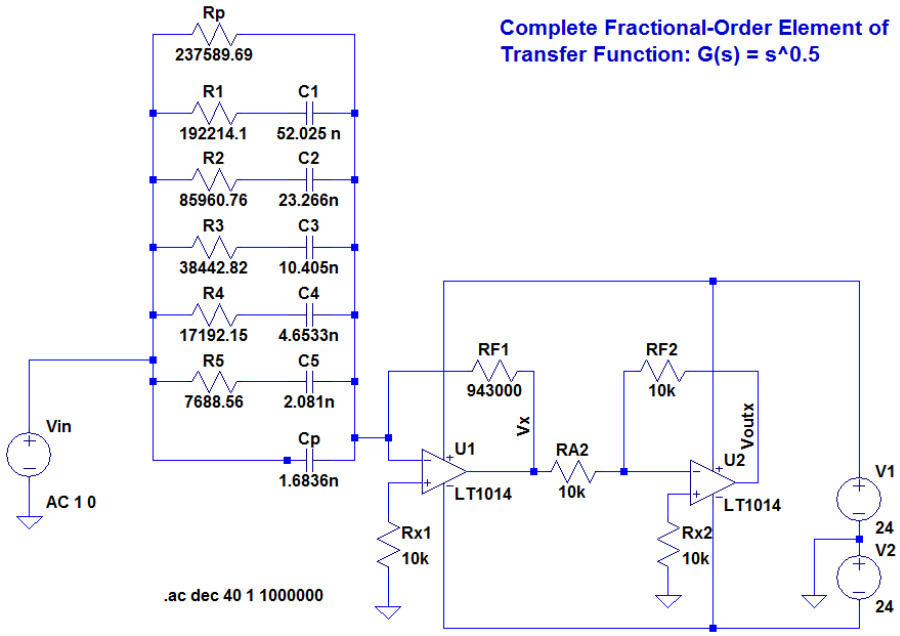

Figure 1. Analog circuit design of a fractional-order differentiator of order $\alpha = 0.5$.

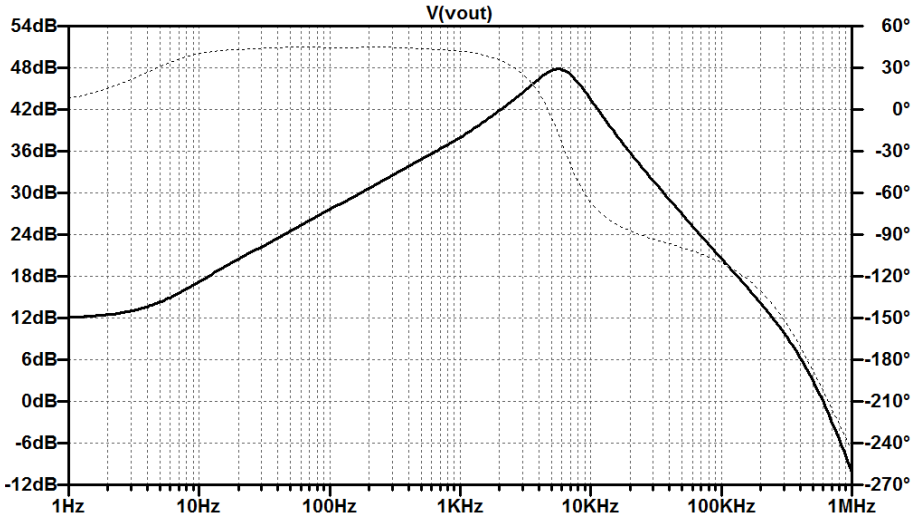

Figure 2. Magnitude (solid line) and phase (dashed line) spectra of a fractional-order differentiator of order $\alpha = 0.5$.

Table I
OP-AMP TRANSISTOR SIZES FOR FIG. 3 USED FOR THE SEMI-DIFFERENTIATOR APPLICATION.

Transistor	Computed Size	Actual Size
M1 and M2	24	24
M3 and M4	15	15
M5	2.8	2.8
M6	283	273.6
M7	26	26
M8	2.8	2.8
M9	0.5936	1

Table II
RESULTING PARAMETERS BASED ON THE OP-AMP DESIGN.

Parameters	Pre-Layout	Post-Layout
Supply, Vdd	1.5 V	1.5 V
Supply, Vss	-1.5 V	-1.5 V
Minimum Length	1 μm	1 μm
Load Capacitance	10 pF	10 pF
Open Loop Gain	76.39 dB	76.39 dB
Phase Margin	57.27°	56.05°
Unity-Gain Bandwidth	22.61 MHz	22.41 MHz
DC Offset	-3.51 μV	-3.573 μV
ICMR	-1.35 to 1.33 V	-1.35 to 1.32 V
Slew Rate	17.87 V/μs	17.84 V/μs
Settling Time	56 ns	56 ns
CMRR	79.76 dB	79.76 dB
PSRR(+)	90.89 dB	90.94 dB
PSRR(-)	94.16 dB	94.16 dB
Power Dissipation	1.23589 mW	1.23650 mW

capacitors. The frequency response of the analog CMOS circuit is shown in Fig. 6 which is similar to the one presented in Fig. 2.

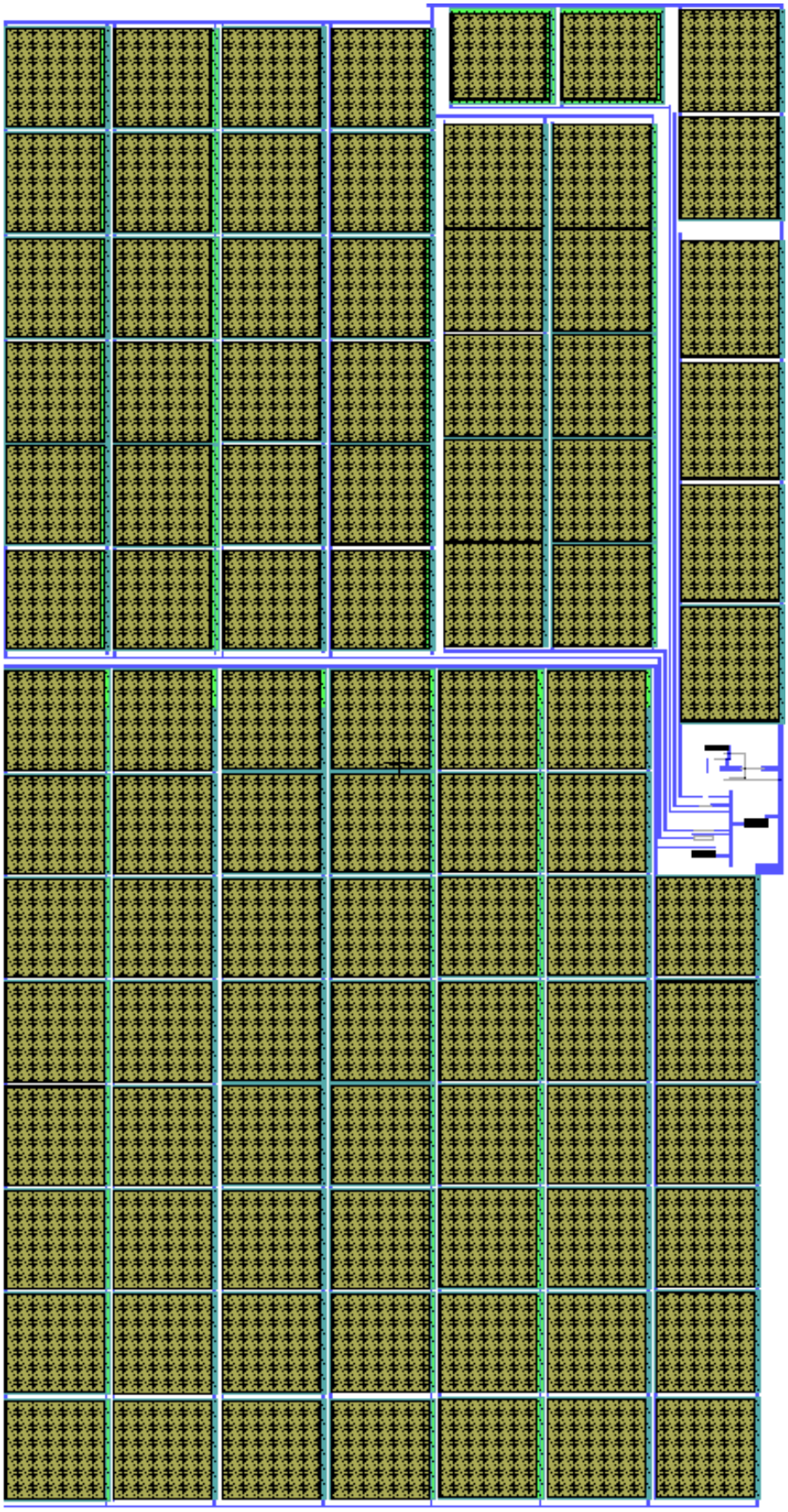

Figure 5. Top-level layout of the semi-differentiator.

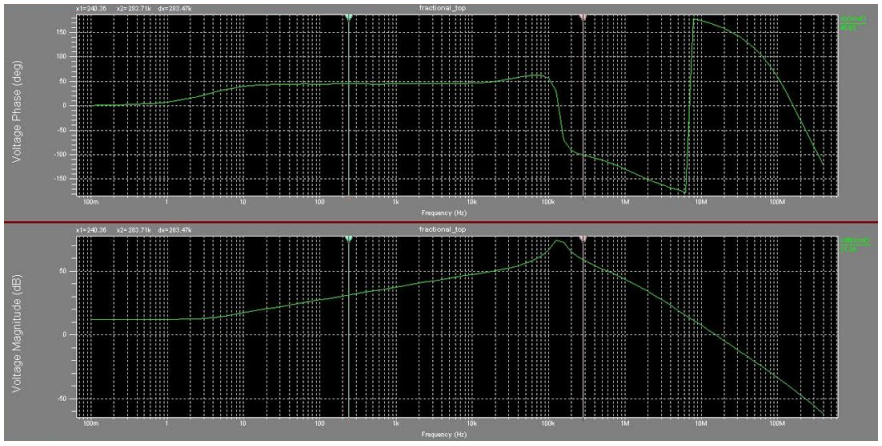

Figure 6. Frequency response of the designed analog CMOS semi-differentiator.

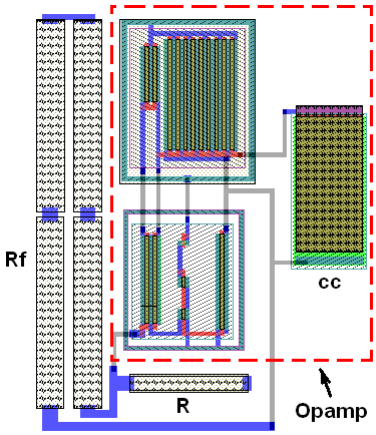

Figure 4. Example layout of an inverting op-amp with a gain of 20.

IV. Conclusion

In this short note, we show that it is possible to realize a fractional-order element (specifically a semi-differentiator) using analog CMOS technology. For the purpose of showing its applicability and for proof of concept, the technology of 0.35-micron was arbitrarily chosen. Simulation results both using solid-state and analog CMOS circuits reveal outstanding similarities from its working bandwidth from 10 kHz to around 10 kHz.

Acknowledgments

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