International Journal of Electronics and Electrical Engineering
ISSN : 2277-7040 Volume 2 Issue 3 (March 2012)
http://www.ijecee.com/ https://sites.google.com/site/ijeceejournal/

Numerical Modeling of Series Resistance of Millimeter-wave DDR IMPATTs

Aritra Acharyya[1, †] and J. P. Banerjee[1],

[1,2]Institute of Radiophysics and Electronics, University of Calcutta, 92, APC Road, Kolkata-712202, West Bengal, India
[†]Corresponding Author: e-mail: ari_besu@yahoo.co.in

Abstract. This paper describes a computer-based method to calculate the parasitic positive series resistance of millimeter-wave packaged DDR IMPATT devices from high-frequency small-signal conductance-susceptance characteristics. The series resistance of the device can be obtained at the threshold condition when the small-signal conductance of the packaged device just becomes negative and the susceptance becomes positive. Series resistance values are determined for two DDR Silicon IMPATT diodes designed to operate at W-band near *94 GHz* window frequency using the method developed by the author's.

Keywords: Conductance-Susceptance Plot, IMPATT Diode, Series Resistance, Small-Signal Analysis.

1 Introduction

The parasitic positive series resistance which originates from the un-swept epitaxial layer (Depletion layer of reverse biased IMPATT diode may not cover the total epitaxial layer; i.e. *p*- or *n*-layer of single drift region or SDR (p^+nn^+ or n^+pp^+) structure or both *p*- and *n*-layer of double drift region or DDR (p^+pnn^+) structure. This uncovered region or inactive region adds undesirable positive parasitic resistance.), package contacts and passive circuit, is a dominant factor which limits output power from an IMPATT source [1-4]. A fraction of microwave power generated within the active layer (within depletion region) will be dissipated as heat in any positive parasitic resistance which will lower the output power from an IMPATT source. The negative resistance of mm-wave IMPATT diode is in the range of only a few ohms. The positive series resistance R_S therefore has to be kept to the minimum possible value by appropriate technology in order to obtain maximum output power from the device. A direct measurement of series resistance R_S by a network analyzer is difficult due to circuit modeling difficulties and network analyzer error. A computer-based method has been developed using accurate values of ionization rates and drift velocities for determination of the series resistance of millimeter wave W-Band packaged DDR IMPATT diode utilizing small-signal conductance-susceptance characteristics at threshold condition (i.e. when the small-signal conductance of the

packaged diode just becomes negative and the susceptance becomes just positive).

Electrical series resistance R_S is well recognized as limiting factor for power and efficiency in IMPATT diodes. An effective indirect method of measuring R_S had been proposed by Michael G. Adlerestein, Lowell H. Holway and Shiou Lung G Chu in 1983 [1]. They used observation of the oscillation threshold bias current for a diode in a standard circuit. The method was applied to GaAs diodes near *40 GHz*. Measurement of R_S for Si IMPATT [Single Drift Region (SDR) Structure] was carried out by M. Mitra, M. Das, S. Kar and S. K. Roy by considering unequal ionization rates and drift velocities of the two types of charge carriers in Silicon in 1994 [2]. In 2009 T. K. Pal of Research Centre Imarat (RCI), Hydrabad, India described a computer-based method to calculate the series resistance of an mm-wave Ka-band packaged IMPATT diode from Small-Signal Conductance-Susceptance characteristics [4]. So several workers has been experimentally measured the parasitic series resistance of IMPATT diodes operating at different frequencies. But the experimental measurement of series resistance is very much time consuming and expensive method. That is why our aim is to develop a generalized computer simulation method capable of predicting the value of parasitic resistance of particular structure of IMPATT diode operating at particular frequency. The numerical modeling of the parasitic resistance must be developed first, which should be independent of operating frequency of the device; that means the model should be consistent at any operating frequency band.

A simulation method for DC and Small-signal analysis of IMPATT devices is presented in this paper; the method is quite generalized and can be applied to any diode structure. The integrated values of microwave device characteristics as well as the contribution of diode negative resistance from individual space step of the depletion layer of the diode can be obtained through use of the method. The method is applied to two Double Drift Region (DDR) structured Continuous wave (CW) Si-IMPATT diodes designed to oscillate in W-Band. This paper mainly describes in detail a computer-based method to calculate the parasitic positive series resistance R_S of millimeter wave W-Band continuous wave packaged DDR IMPATT diodes from high frequency small signal conductance-susceptance characteristics. This method would be suitable for determining R_S for mm-wave diodes with appropriate values of ionization rate ratios at maximum electric field. R_S values are determined for two DDR Si-IMPATT diodes designed to operate in W-Band by the author's developed method.

2 Method to Estimate Series Resistance Numerically

An equivalent circuit representation of IMPATT diode with package is shown in Fig. 1 [5], where G and B are the diode conductance and susceptance respectively. The magnitudes of G and B are obtained from simulation by using realistic values of ionization rate and drift velocities of charge carriers in Silicon at 500 K [6-8]. R_S is

the series resistance of the device, g is the load conductance and L is the circuit inductance. C_p and L_p are the package capacitance and package inductance respectively. Impedance of the packaged device is given by,

$$Z_{DP} = \frac{1}{G + j(B - B_P)} + R_S = \frac{G + R_S G^2 + R_S (B - B_P)^2 - j(B - B_P)}{G^2 + (B - B_P)^2} \quad (1)$$

Where, $B_P = \dfrac{1}{\left(\omega L_P - \dfrac{1}{\omega C_P}\right)}$ = Effective susceptance caused by package-parameters.

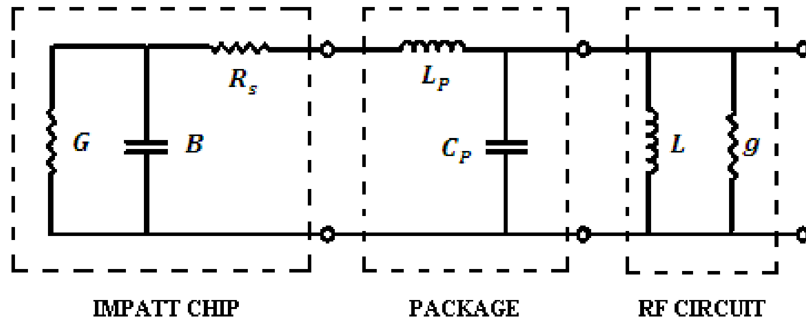

Fig. 2. Equivalent model of Packaged IMPATT diode [5].

Impedance of the RF circuit is given by,

$$Z_{RF} = \frac{j\omega L\left(\frac{1}{g}\right)}{\frac{1}{g} + j\omega L} = \frac{\omega^2 L^2 g + j\omega L}{1 + \omega^2 L^2 g^2} \quad (2)$$

In a practical oscillator circuit, the steady-state condition for oscillation is given by,

$$Z_{DP} + Z_{RF} = 0 \quad (3)$$

Both real and imaginary parts of equation (3) must be separately equal to zero,

$$Real(Z_{DP} + Z_{RF}) = 0 \quad (4)$$

$$Imaginary(Z_{DP} + Z_{RF}) = 0 \quad (5)$$

From equation (5) we get,

$$\frac{G + R_S G^2 + R_S (B - B_P)^2}{G^2 + (B - B_P)^2} + \frac{\omega^2 L^2 g}{1 + \omega^2 L^2 g} = 0 \quad (6)$$

At the threshold condition, the device negative conductance is much larger than the positive conductance of RF circuit and so the oscillation builds up. The oscillation is started by a random noise fluctuation which grows when the total conductance of the device-circuit system is negative. For stability of oscillation it is necessary that as the oscillation amplitude grows the magnitude of the negative conductance of the active

device tends to decrease. This is shown to be the case, for IMPATT oscillator by Scharfetter and Gummel [9], where the authors have shown that with increasing voltage swing, the susceptance of the diode remains almost constant. Thus the frequency of oscillation does not change much with the buildup of amplitude of oscillation. The oscillation continues to build up for several cycles until the magnitude of the device negative conductance decreases to the value of positive conductance of the load. The oscillation then becomes stable. In the practical case, it is a good approximation to take $g = 0$ at the oscillation threshold. Then equation (7) reduces to,

$$G_{th} + R_S G_{th}^2 + R_S (B_{th} - B_P)^2 = 0 \tag{8}$$

Where, G_{th} is small signal conductance of the diode at the threshold condition when the total conductance of the packaged diode becomes just negative. B_{th} is the small signal threshold susceptance of the diode, corresponding to the threshold conductance G_{th}. Considering the package inductance L_P and package capacitance C_P, the equivalent circuit of the IMPATT diode with package parameter is shown in Fig. 2 and the expression for series resistance, R_S is modified to,

$$R_S = \frac{|G_{th}|}{\left[G_{th}^2 + (B_{th} - B_P)^2\right]} \tag{9}$$

3 Results and Discussion

Two Silicon based Double Drift Region (DDR) IMPATT diodes are designed and optimized for CW operation within W-Band using Sze and Ryder formula [0] and DC and small-signal simulation method proposed by Roy et al. [11-12] based on Gummel-Blue approach [13]. Simulation studies are carried out for doping and structural parameters listed in Table 2. The whole computer simulation is carried out using MATLAB 7 software. Necessary device and package parameters for W-Band are tabulated in Table 1.

The following assumptions are made in DC and small-signal computer analysis of IMPATT diodes. (a) One dimensional model of *p-n* junction has been considered, (b) The electron and hole velocities have been taken to be saturated and independent of electric field throughout the space charge layer, and (c) Carrier diffusion has been neglected. In this method the computation starts from the field maximum near the metallurgical junction. The distribution of the electric field and carrier currents in the depletion layer are obtained by the double-iterative computer method, which involves iteration over the magnitude of field maximum and its location in the depletion layer.

Simulated results of DC and high frequency (small-signal) properties of two DDR CW Si-IMPATT diodes are listed in Table-3. Efficiency of DDR-1 is about 10.07% and that of DDR-2 is 13.61% which are not so high in 98 GHz and 95 GHz respectively. RF power outputs of those devices are also very low due to continuous wave operation. Fig. 3 and Fig. 4 depict the electric field profiles of DDR-1 and

International Journal of Electronics and Electrical Engineering
ISSN : 2277-7040 Volume 2 Issue 3 (March 2012)
http://www.ijecee.com/ https://sites.google.com/site/ijeceejournal/

DDR-2 respectively. Electric-field profiles will distort due if the current density increased as a result of the space charge effect. Fig. 5 and Fig. 6 depict the small-signal Conductance-Susceptance plots of DDR-1 and DDR-2 respectively.

Similarly negative resistance distributions as a function of distance for DDR-1 and DDR-2 are shown in Fig. 7 and Fig. 8 respectively. It can be observed from those plots that magnitude of the peak resistance is larger at n-side than that of p-side. It is due to in case of silicon average ionization rate of electrons is much higher than that of holes. Quality factors, ($Q = -B/G$ at peak frequency) of the diodes DDR-1 and DDR-2 can be calculated as 3.81 and 3.34 respectively from Table 3.

TABLE 1: DEVICE AND PACKAGE PARAMETERS FOR THE W-BAND

PARAMETER	VALUE
TEMPERATURE (K)	*500*
CW DIODE JUNCTION DIAMETER, D_j (μm)	*35*
PACKAGE INDUCTANCE, L_P (nH)	*0.05*
PACKAGE CAPACITANCE, C_P (pF)	*0.13*

TABLE 2: STRUCTURAL AND DOPING PARAMETERS FOR CONTINUOUS WAVE W-BAND SI-IMPATT DIODES

PARAMETER	DDR-1	DDR-2
n-epitaxial layer doping concentration ($\times 10^{23}$ m^{-3})	1.400	1.000
p-epitaxial layer doping concentration ($\times 10^{23}$ m^{-3})	1.700	1.500
n^{+}-substrate doping concentration ($\times 10^{26}$ m^{-3})	1.000	1.000
Width of the n-layer (μm)	0.400	0.420
Width of the p-layer (μm)	0.300	0.380

TABLE 3: DC AND SMALL-SIGNAL ANALYSIS OF CONTINUOUS WAVE DDR SI-IMPATT DIODES WITHIN W-BAND

PARAMETERS	DDR-1	DDR-2
Current Density, J_0 (Amp/ m^2)	6.00×10^8	4.50×10^8
Peak Electric Field, ξ_m (V/m)	6.20×10^7	5.78×10^7
Breakdown Voltage, V_B (V)	21.98	28.28
Efficiency, η (%)	10.07	13.61
Peak Negative Conductance, (Sm/m^2)	-26.05×10^6	-30.20×10^6
Peak Positive Susceptance, (Sm/m^2)	99.27×10^6	100.95×10^6
Quality Factor, Q	3.81	3.34
Negative Resistance at Peak Frequency ($\times10^{-8}$ Ohm/m^2)	-0.2473	-0.2720
Peak Operating Frequency, f_{opt} (GHz)	98.0	95.0
Threshold Frequency, f_{th} (GHz)	75.5	74.0
RF Power Output ($Watts$)	0.157	0.302

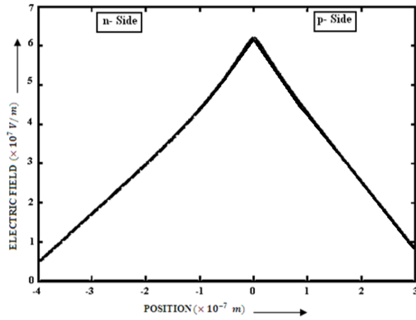

Fig. 3. Electric Field Profile of DDR-1.

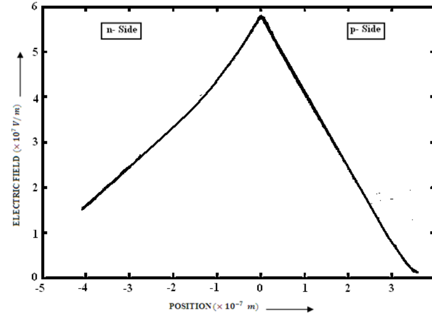

Fig. 4. Electric Field Profile of DDR-2.

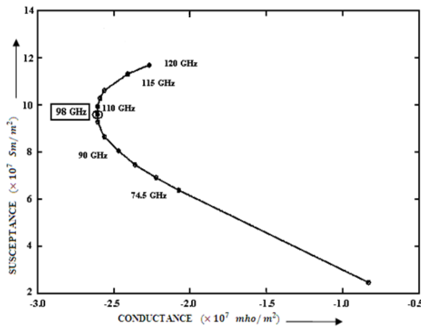

Fig. 5. Small-Signal Conductance-Susceptance plot of DDR-1.

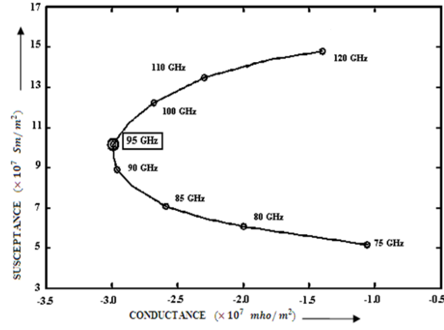

Fig. 6. Small-Signal Conductance-Susceptance plot of DDR-2.

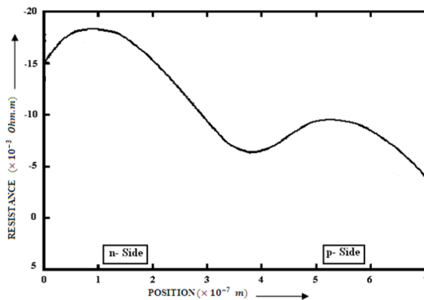

Fig. 7. Negative Resistance Profile of DDR-1.

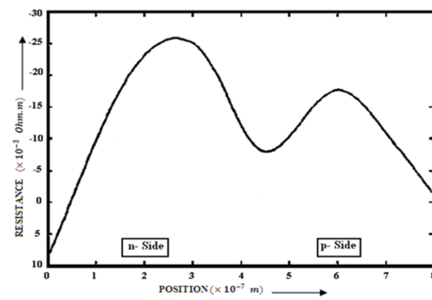

Fig. 8. Negative Resistance Profile of DDR-2.

International Journal of Electronics and Electrical Engineering
ISSN : 2277-7040 Volume 2 Issue 3 (March 2012)
http://www.ijecee.com/ https://sites.google.com/site/ijeceejournal/

Now the series resistances of the diodes are calculated utilizing small-signal conductance-susceptance plots at threshold condition using (30). Variation of series resistances with current densities are shown in Fig. 9 and Fig.10 for DDR-1 and DDR-2 respectively. From those plots it can be observed that the variations of series resistances are minor with respect to current density for both the diodes. Fig. 9 and Fig. 10 show a very small positive slope of series resistance vs current density curves. This positive slope of linear variation of series resistance against current density can be explained from modified Alderstein expression [1-2, 4],

$$R_s = \left(\frac{[d_n d(c+1) I_{th}]}{[0.74\pi^4 (d+1) f_{th}{}^2 C_d{}^2]} \right) \left(\frac{f_{opt}}{f_{th}} \right) \quad (10)$$

Where, d_n is the derivative of the electron ionization rate with respect to electric field; I_{th} is the threshold current at which the oscillation just starts; f_{th} and f_{opt} are experimentally measured threshold and optimum frequency respectively; and C_d is the device capacitance. And $c = \alpha_p/\alpha_n$ and $d = v_p/v_n$; where α_p, α_n, v_p, v_n are the electron and hole ionization rates and drift velocities at the maximum field point in the depletion layer respectively. From equation (31) it is clear that the series resistance is directly proportional to the threshold current (I_{th}). But in practice this dependence is very small. That is way series resistance varies linearly with current density with a very small positive slope.

Series Resistance of IMPATT devices originates from un-depleted epitaxial layers, package contacts and diode circuits. Effect of package is already taken into account in this analysis. Now the value of parasitic positive series resistance of the device also depends on the conductivity of the substrate layer (n^+-substrate). As the conductivity of the substrate increased the amount of contribution of the substrate-positive resistance (which is decreased due to increment of the conductivity) over total series resistance decreased. Consequently the total series resistance of the device decreased. Dependence of the series resistance over substrate doping for DDR-1 and DDR-2 are depicted in Fig. 11 and Fig. 12 respectively.

Since the doping concentration of n^+-substrate layer is very high ($10^{25} – 10^{26}\ m^{-3}$), conductivity of this layer is very high. Generally for W-Band Si DDR IMPATT diodes the thickness of the substrate layer is very small (*200 nm – 500 nm*). That is why the total contribution of the substrate layer series resistance on total series resistance of the diode is very small. This is the cause of very minor variation of R_S against substrate doping concentration.

Finally our simulation predicted series resistance values are compared with published experimental results. Unfortunately experimental studies on series resistance of W-band Silicon DDR IMPATT diodes are not reported yet in any existing published literature. That's why we have to compare our results with experimentally obtained series resistance values of SDR diodes operating at lower frequencies and lower current densities. Since results show a very small dependence of series resistance on current density, that's why this comparison is almost valid.

From the Table 4 it can be observed that the X-band and Ka-band diodes posses much larger values of series resistance than the W-band diodes (DDR-1 & DDR-2). This fact can be explained in the following way. The frequency of operation of an

IMPATT diode essentially depends on the transit time of charge carriers to cross the depletion layer of the diode. IMPATT diodes can be roughly designed by using the transit time formula of Sze and Ryder [10] which is $W_{n,p} = 0.37\ v_{sn,sp} / f$; where $W_{n,p}$, $v_{sn,sp}$ and f are the total depletion layer width (n or p-side), saturation velocity of electrons/holes and operating frequency respectively. From Sze and Ryder formula it is clear that higher frequency of operation means shorted thickness of epitaxial layer. Shorter thickness of epitaxial layer means obviously shorter thickness of un-depleted inactive layer which is mainly responsible for positive parasitic series resistance of the device. That means higher frequency diode should have smaller series resistance. This is the probable cause of simulation predicted smaller values of series resistance of W-Band diodes compared to lower frequency (X-Band and Ka-Band) diodes.

TABLE 4: COMPARISON OF SIMULATION RESULTS WITH EXPERIMENTAL PUBLISHED DATA

PARAMETERS	SIMULATION RESULTS		EXPERIMENTAL RESULTS	
	DDR-1	**DDR-2**	**Ka-Band (Experimented by Pal T. K., 2009 [4])**	**X-Band (Experimented by Mitra M. *et al.*, 1993 [2])**
Operating Frequency (GHz)	98	95	35.3	11.651
Bias Current Density, J_0 (Am^{-2})	6.00×10^{8}	4.50×10^{8}	0.84×10^{8}	0.26×10^{8}
Breakdown Voltage, V_B (V)	21.98	28.28	45	-
Efficiency, η (%)	10.07	13.61	-	-
Series Resistance, R_S (Ohm)	0.8702	0.6734	1.0380	1.4400

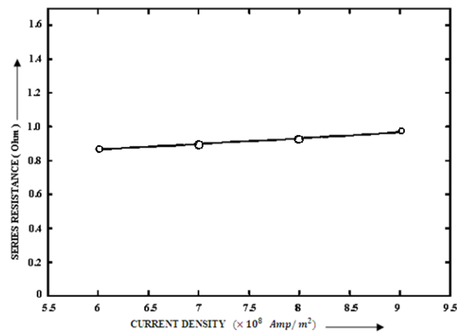

Fig. 9. Series Resistance vs Current Density Plot of DDR-1.

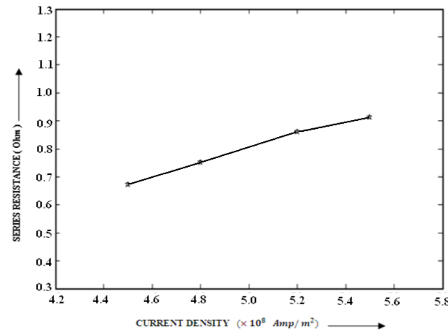

Fig. 10. Series Resistance vs Current Density Plot of DDR-2.

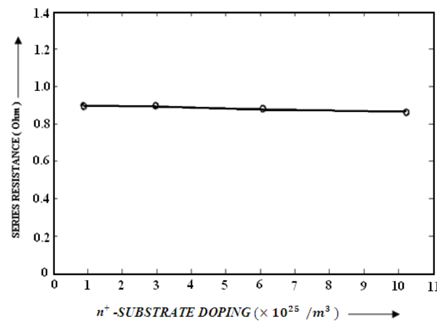

Fig. 11. Series Resistance vs Substrate Doping Plot for DDR-1.

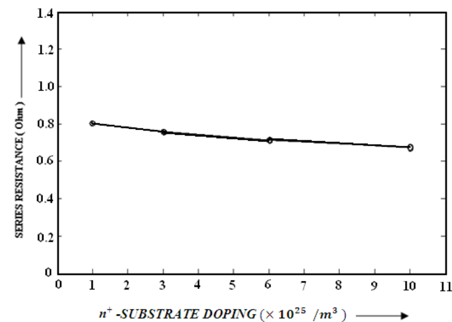

Fig. 12. Series Resistance vs Substrate Doping Plot for DDR-2.

4 Conclusions

A computer-based method for determination of the series resistance of millimeter wave W-band DDR IMPATT diodes have been presented in this paper. The method requires the values of threshold conductance G_{th}, susceptance B_{th} of the packaged diode, which can be obtained from the well established small-signal study, and the values of package parameters L_P and C_P from direct measurement or manufacturer's data. The method should also be applicable to the higher millimeter wave frequency bands, since the basic conditions chosen are the low-power, low-current oscillation threshold where small signal analysis holds good.

References

1. Adlerestein, M. G., Holway, L. G., and Chu, S. L. G.: Measurement of Series Resistance in IMPATT Diode, IEEE Trans. Electron Devices, vol. ED-30, pp. 179--182, (1983).
2. Mitra, M., Das M., Kar, S. and Roy, S. K.: A Study of the Electrical Series Resistance of Silicon IMPATT Diodes, IEEE Trans. Electron Devices, vol. ED-40, pp. 1890--1893, (1993).
3. Roy, U. C., Gupta, A. K.: Measurement of electrical series resistance of W-band Si IMPATT diode, *Proc. 2nd Asia-Pacific Microwave Conf., Bejing, China*, (1988).
4. Pal, T. K.: Series Resistance of Silicon Millimeter Wave (Ka-Band) IMPATT Diodes, *Defence Science Journal, India*, vol. 59, no. 2, pp. 1--5, (2009).
5. Brooker, G.M.: Long-range Imaging Radar for Autonomous Navigation, Ph.D. dissertation, University of Sydney. Aerospace, Mechanical and Mechatronic Engineering, pp. 231, (2006).
6. Grant, W. N.: Electron and hole ionization rates in epitaxial Silicon, *Solid State Electron*, vol. 16, pp. 1189--1203, (1973).

7. Canali, C., Ottaviani, G. and Quaranta A. A.: Drift velocity of electrons and holes and associated anisotropic effects in silicon, *J. Phys. Chem. Solids*, vol. 32, no. 8, pp. 1707, (1971).
8. "Electronic Archive: New Semiconductor Materials, Characteristics and Properties", http://www.ioffe.ru/SVA/NSM/Semicond.
9. Scharfetter, D. L. and Gummel, H. K.: Large-Signal Analysis of a Silicon Read Diode Oscillator, *IEEE Trans. on Electron Devices*, vol. ED 16, no. 1, pp. 64--77, (1969).
10. Sze, S. M., and Ryder, R. M.: Microwave Avalanche Diodes, *Proc. of IEEE, Special Issue on Microwave Semiconductor Devices*, vol. 59, issue 8, pp. 1140--1154, (1971).
11. Roy, S. K., Sridharan, M., Ghosh, R. and Pal, B. B.: Computer method for the dc field and carrier current profiles in the IMPATT device starting from the field extremum in the depletion layer, *Proceedings of the 1st Conference on Numerical Analysis of Semiconductor Devices (NASECODE I), J. H. Miller, Ed., Dublin, Ireland*, pp. 266--274, (1979).
12. Roy, S. K., Banerjee, J. P. and Pati, S. P.: A Computer analysis of the distribution of high frequency negative resistance in the depletion layer of IMPATT Diodes, *Proc. 4th Conf. on Num. Anal. of Semiconductor Devices (NASECODE IV) (Dublin) (Dublin: Boole)*, pp. 494--500, (1985).
13. Gummel, H. K. and Blue, J. L.: A small-signal theory of avalanche noise in IMPATT diodes, *IEEE Trans. on Electron Devices*, vol. ED-14, no. 9, pp. 569--580, (1967).