The Mythology of the Memristor

Blaise Mouttet
George Mason University
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Myth #1

The memristor is the "4th fundamental circuit element"

Memristor Reductio Ad Absurdum

4 relationships

$q, i \longleftrightarrow \phi, v$

9 relationships

$q, i, di/dt \longleftrightarrow \phi, v, dv/dt$

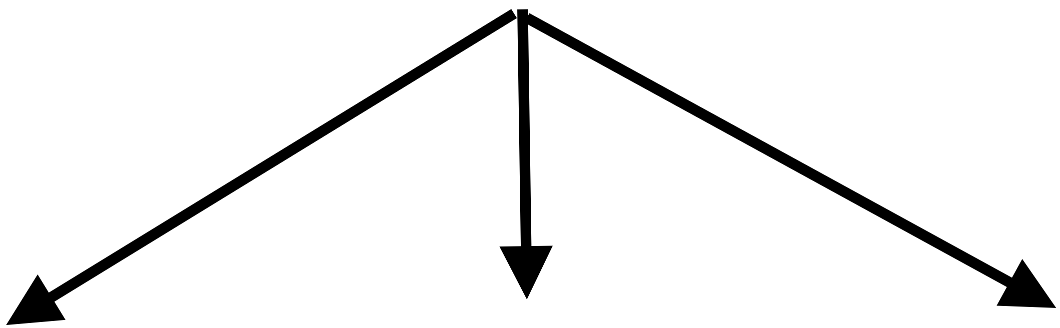
16 relationships

$q, i, di/dt, d^2i/dt^2 \longleftrightarrow \phi, v, dv/dt, d^2v/dt^2$

⋮

Memristor/Resistor are both special cases of the same system

$$v = R(w)\, i$$



$dw/dt = 0$ (linear resistor)

$dw/dt = i$ (memristor)

$dw/dt = di/dt$ (non-linear resistor)

Are mem-capacitor and mem-inductor the 5th and 6th "fundamental" circuit elements?

Memristive System(1976):

$$v = R(w,i,t)\, i$$

$$dw/dt = f_R(w,i,t)$$

Memcapacitive System(2009):

$$q = C(w,v,t)\, v$$

$$dw/dt = f_C(w,v,t)$$

Meminductive System(2009):

$$\varphi = L(w,i,t)\, i$$

$$dw/dt = f_L(w,i,t)$$

M. DiVentra, Y. V. Pershin, L.O. Chua, "Putting Memory into Circuit Elements: Memristors, Memcapacitors, and Meminductors," Proceedings of the IEEE, vol 97, iss.8, (2009)

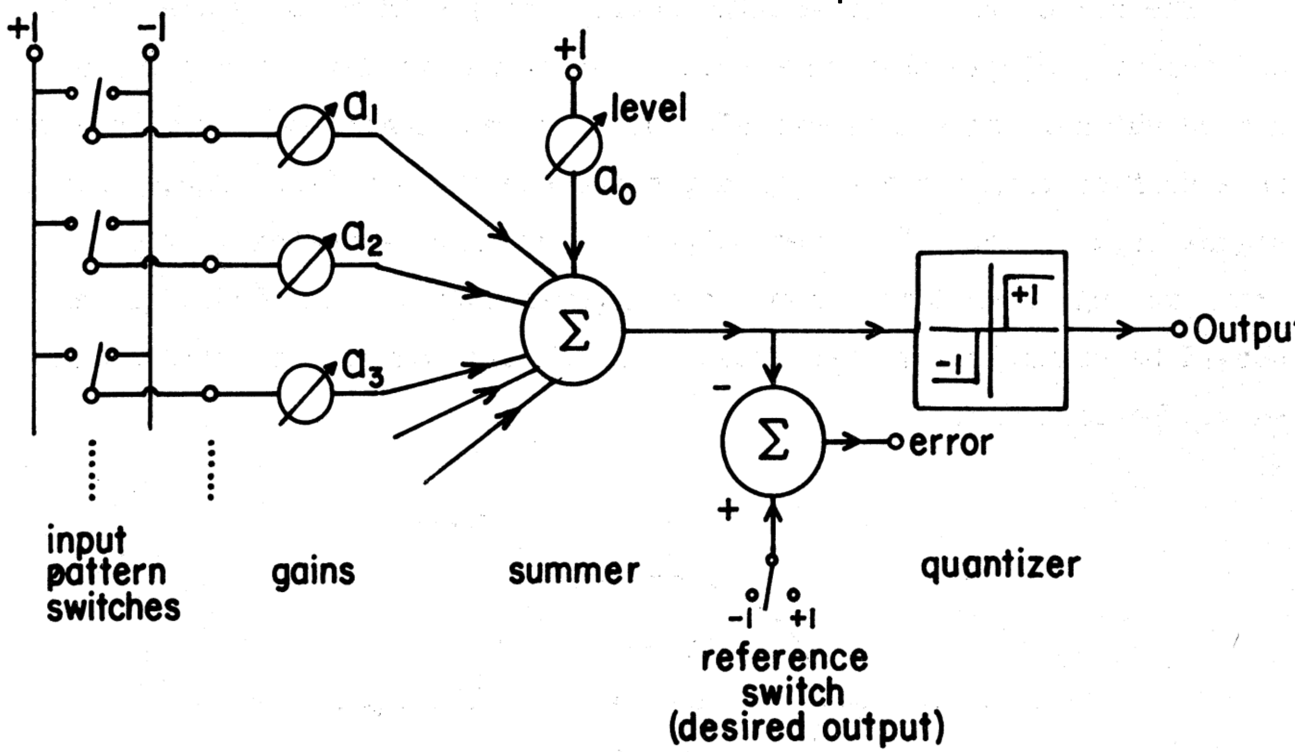
Myth#2

HPLabs “found” the “missing” memristor.

Bernard Widrow's ADALINE circuit (1960)

(ADALINE = adaptive linear neuron)

a_i = memistors



Bernard Widrow's memistor = 3-terminal memristor

*"Like the transistor, the **memistor** is a 3-terminal element. The **conductance** between two of the terminals is **controlled by the time integral of the current** in the third, rather than its instantaneous value as in the transistor."*

-Widrow et al.[1] (1961)

[1]Widrow et al., "Birth, Life, and Death in Microelectronic Systems," Office of Naval Research Technical Report 1552-2/1851-1, May 30,1961

Additional Memistor References

- A.O.Bondar et al., “Simulation of the plasticity of synapses using memistors,” *Sov. Automat. Contr.*, n.6, p47-51, 1968.
- S.Thakoor et al., “Solid-state thin-film memistor for electronic neural networks,” *Journal of Applied Physics*, v.67, n.6, 1990.
- G.Shen et al., “Fabrication and performance of solid-state thin-film memistor,” *Vacuum Science and Technology*, v.18,n.8, 1998.

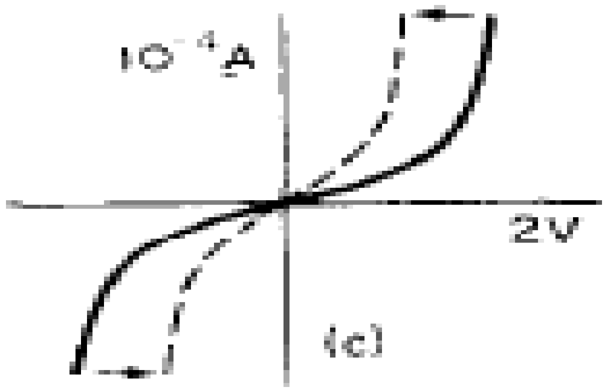
Solid-State Electronics Pergamon Press 1968. Vol. 11, pp. 535–541. Printed in Great Britain

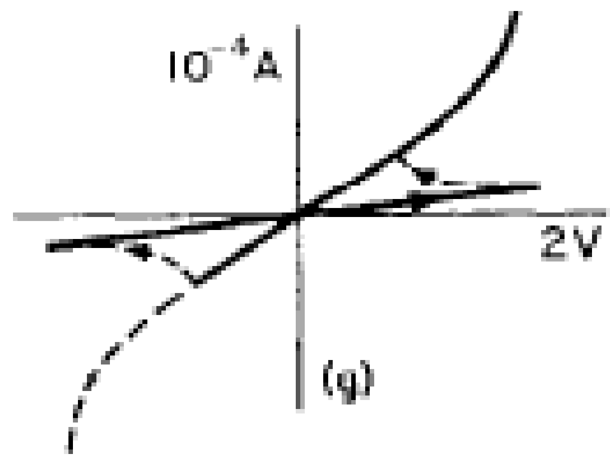
SWITCHING PHENOMENA IN TITANIUM OXIDE THIN FILMS

F. ARGALL

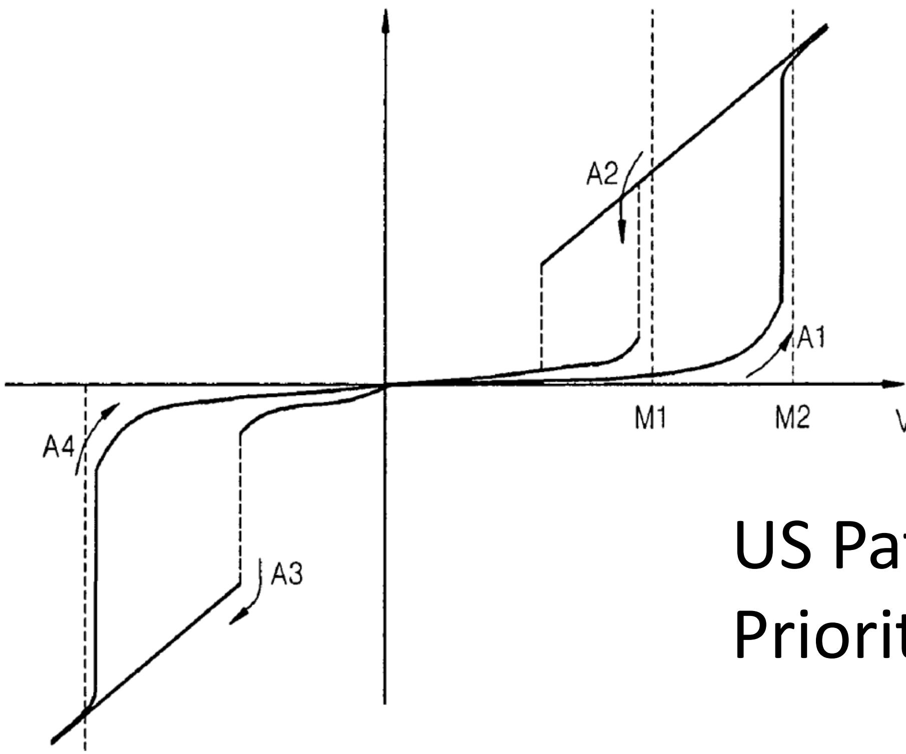
Physics Department, Chelsea College of Science and Technology, University of London, London, S.W.3

(*Received 27 July* 1967)





Samsung (not HP) holds basic U.S. patent for TiO_{2-x}/TiO_2 resistance memory[1]



US Patent 7,417,271 (Fig. 4), Priority Feb. 27, 2006

[1]Genrikh et al., "Electrode structure having at least two oxide layers and non-volatile memory device having the same," US Patent 7,417,271, priority Feb 27, 2006

Samsung (not HP) holds basic U.S. patent for TiO_{2-x}/TiO_2 resistance memory[1]

Claim 1-
An electrode structure, comprising:
a lower electrode;
a first oxide layer formed on the lower electrode,
wherein **the first oxide layer** is formed of an oxide having **a variable oxidation state**;
a second oxide layer formed on the first oxide layer; and
an upper electrode formed on the second oxide layer,
wherein at least one of the first and second oxide layers are formed of **a resistance-varying material**.

[1]Genrikh et al., "Electrode structure having at least two oxide layers and non-volatile memory device having the same," US Patent 7,417,271, priority Feb 27, 2006

HP's "memristor" is not actually a true memristor!

Mathematical definition of a true memristor:

1) $v = R(w)\, i$ 2) $dw/dt = i$

HP's TiO_{2-x}/TiO_2 "memristor"[1]:

$$\dot{w} = f_{\text{on}} \sinh\left(\frac{i}{i_{\text{on}}}\right) \exp\left[-\exp\left(-\frac{w - a_{\text{on}}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right]$$

[1]M.D. Pickett et al., "Switching dynamics in titanium dioxide memristive devices," Journal of Applied Physics, 106, 074508, (2009)

Inconsistencies between memristor theory and physics of MIM thin films

1) v=R(w)i is insufficient to account for Schottky junctions, charge trapping , electroforming , etc.
2) dw/dt ≠ i due to non-linearity of ionic mobility[1] and/or tunneling[2] effects.
3) MIM junctions are capacitive. This is not properly accounted for by the proposed memristive systems models.

[1]D.B. Strukov, R.S. Williams, "Exponential ionic drift: fast switching and low volatility of thin film memristors," Applied Physics A, 94:515-519, (2009)
[2]M.D. Pickett et al., "Switching dynamics in titanium dioxide memristive devices," Journal of Applied Physics, 106, 074508, (2009)

Myth#3

Memristive memory will replace Flash/SRAM/DRAM.

- Non-volatile memory (and FPGA) are mature multi-billion dollar markets – not good for any radical innovation. Scaling will likely continue with multi-gate and/or high-k oxide solutions.
- Samsung, Intel, STMicroelectronics, and Micron (Numonyx) are all supporting phase change memory as next-gen NVM not memristors.
- Unity Semiconductor has been developing prototype metal oxide RRAM since 2002 but they do not consider their devices memristors.
- HPLabs had (until about 2006) been developing molecular (not metal oxide) memory. HP does not have the fab experience or ability for large scale non-volatile memory fabrication and have zero patents covering metal oxide RRAM.

Distribution of U.S. Patents Claiming Types of Memory Resistance Materials

	Metal Oxide	Solid Electrolyte	Phase Change	Molecular
AMD	0	0	0	12
Axon Technology	0	20	0	0
Hewlett Packard	0	0	0	36
Micron	0	0	106	0
Samsung	4	0	10	0
Sharp	18	0	0	0
Unity Semi	6	0	0	0

Conclusions

- The interpretation of the memristor as the "fourth fundamental circuit element" is misguided (although more generalized memristive systems might be useful for RRAM modeling).
- HP's claiming credit for finding the "missing" memristor is a successful PR stunt but does not withstand scrutiny.
- Non-volatile memory market seems unlikely to be impacted by memristor. Phase change memory appears to be gaining more industry support.