Pinched hysteresis loops are a fingerprint of square law capacitors

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Abstract— **It has been claimed that pinched hysteresis curves are the fingerprint of memristors. This paper demonstrates that a linear resistor in parallel with a nonlinear, square law capacitor also produces pinched hysteresis curves. Spice simulations are performed examining the current vs. voltage behavior of this circuitry under different amplitudes and frequencies of an input signal. Based on this finding a more generalized dynamic systems model is suggested for ReRAM and neuromorphic modeling to cover a broader range of pinched hysteresis curves.**

Keywords- non-linear circuit theory, RRAM, ReRAM, memristor, memristive systems, memadmittance systems, memresistor

I. INTRODUCTION

It has been argued that the memristor should be considered a fundamental non-linear circuit element based on the inability to replicate memristor properties by a combination of resistors, capacitors, and inductors [1-2]. More recently it was suggested that pinched hysteresis is a defining property of memristors [3]. Others have claimed pinched hysteresis of TiO_2 thin films as sufficient proof for the discovery of a memristor [4] and have used the pinched hysteresis definition to suggest that ReRAM, phase change memory, and MRAM should also be considered memristors [5]. Several examples of dynamic systems capable of producing pinched hysteresis curves and yet falling outside of the definition of the memristor or memristive systems have also been shown [6-8]. It has been argued that some of these examples include pinched hysteresis loops sensitive to initial condition, amplitude, and frequency variations [9]. As explained in [10] this argument supports the position that the memristor and memristive systems represent incomplete models for ReRAM since the pinched hysteresis of TiO_2 thin film resistance switches have been shown to be sensitive to initial conditions (e.g., Fig. 1a of [11]). Other dynamic systems models for ReRAM have also been considered [12].

This paper demonstrates that a pinched hysteresis effect can be generated using a linear resistor and a nonlinear capacitor. Based on this finding a more generalized dynamic systems model is suggested for ReRAM and neuromorphic modeling of memory resistors.

II. SQUARE LAW CAPACITOR MODEL

An ideal linear capacitor is defined based upon a proportional relationship between electric charge q_c and an applied voltage v. A square law (nonlinear) capacitor is proposed based upon a proportional relationship between electric charge q_c and the square of an applied voltage v such that

$$q_c(t) = C_v v^2(t) \tag{1}$$

where C_v is a proportionality constant having units of farads/volt. Differentiating (1) produces a relationship between the capacitive current ($i_c = dq_c/dt$) and voltage v.

$$i_c(t) = 2C_v v(t) \frac{dv(t)}{dt} \tag{2}$$

Based on Kirchoff's current law placing a square law capacitor in parallel with a linear resistor produces a total current i_T equal to the sum of the resistor current i_R and the capacitive current i_C.

$$i_T(t) = i_R(t) + i_C(t) \tag{3}$$

This equation can be expressed in terms of voltage using (2) combined with Ohm's law with R equal to the resistance.

$$i_T(t) = \frac{1}{R}v(t) + 2C_v v(t)\frac{dv(t)}{dt} \qquad (4)$$

The voltage term $v(t)$ can then be factored out producing

$$i_T(t) = \left(\frac{1}{R} + 2C_v\frac{dv(t)}{dt}\right)v(t) \qquad (5)$$

Substituting a sinusoidal applied voltage with amplitude V_m and frequency f (i.e. $v(t) = V_m\sin(2\pi ft)$) into (5) produces

$$i_T(t) = \left(\frac{V_m}{R} + 4\pi f C_v {V_m}^2\cos(2\pi ft)\right)\sin(2\pi ft) \qquad (6)$$

It is noted that based on (5) $v(t)=0$ implies $i_T(t)=0$. It is also noted that based on (6) for the voltage and the current to be the same sign (positive or negative) the following inequality must hold.

$$\frac{V_m}{R} + 4\pi f C_v {V_m}^2\cos(2\pi ft) \geq 0 \qquad (7)$$

Since the minimum value of cos(ωt) is -1 the signal voltage has an upper bound.

$$V_m \leq \frac{1}{4\pi f R C_v} \qquad (8)$$

The following section provides results of a circuit simulation of the above described square law capacitor in parallel with a linear resistor.

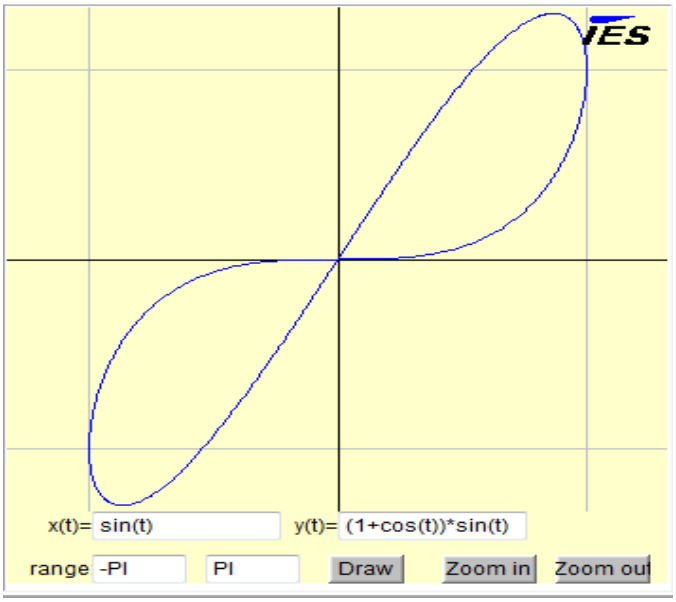
III. CIRCUIT SIMULATION

The following examples were simulated using LTSpice IV based on a linear resistor in parallel with a square law capacitor (see page 5). Lissajous curves were modeled using an online parametric graphing tool [13] based on equation (6).

Example 1 (R=5kΩ, C_v=0.5μF/V, f=200Hz, V_m=0.159V)

For the values of this example equation (6) reduces to

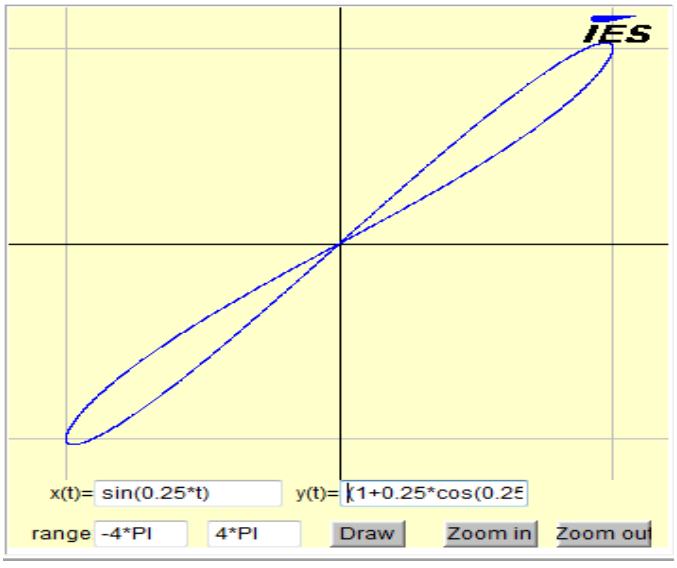
$$i_T(t) = 31.8\mu A(1 + \cos(400\pi t))\sin(400\pi t) \qquad (9)$$



The signal amplitude V_m was selected to be the maximum value of equation (8) so that the sign of the current is always the same as the sign of the voltage.

Example 2 (R=5kΩ, C_v=0.5μF/V, f=50Hz, V_m=0.159V)

$$i_T(t) = 31.8\mu A(1 + 0.25\cos(100\pi t))\sin(100\pi t) \qquad (10)$$

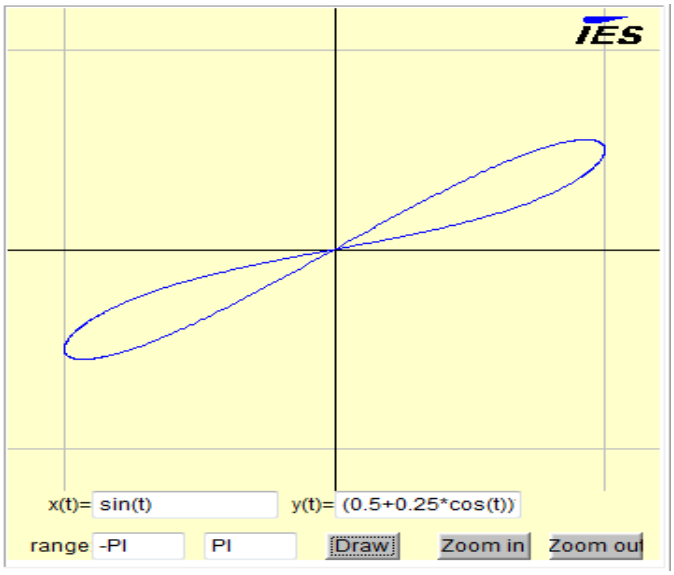


In this example the frequency was reduced to 25% of that in Example 1. The hysteresis curve begins to degenerate as the frequency is reduced and, as

evident from (6), at zero frequency the circuit becomes purely resistive. This behavior may be useful to distinguish a square law capacitor from the theoretical memristor in which decreasing the frequency would increase the hysteresis effect.

Example 3 (R=5kΩ, C_v=0.5μF/V, f=200Hz, V_m=0.0795V)

$$i_T(t) = 31.8\mu A(0.5 + 0.25\cos(400\pi t))\sin(400\pi t) \quad (11)$$



In this example the voltage amplitude is reduced to half of that in Example 1. The hysteresis curve begins to degenerate as the amplitude is reduced similarly to the behavior of the theoretical memristor.

IV. GENERALIZED MEMADMITTANCE SYSTEMS

The theoretical concept of an ideal square law capacitor may be difficult (perhaps impossible) to recreate in real physical systems. It might be possible to construct a device that oscillates between positive and negative capacitance having a zero capacitance at zero voltage. But even if this is possible a more general model than square law capacitance is likely to be necessary to capture the dynamics of such systems. A generalized non-linear version of (4) is proposed as

$$i_T(t) = i_R(v(t)) + C(v(t))\frac{dv(t)}{dt} \quad (12)$$

where $i_R(v(t))$ is a continuous function of voltage $v(t)$ representing the resistive current and $C(v(t))$ is a continuous function of voltage $v(t)$ representing the capacitance. The zero-crossing property will be preserved provided that $i_R(0)=0$ and $C(0)=0$.

In order to model ReRAM and other electronic devices exhibiting memory effects, equation (12) needs to be further generalized as a memadmittance system [14]. This may be achieved by including a dependence on state variables for the resistive current and capacitive functions in which the state variables are defined by differential equations. A state-space representation of this generalization is given as

$$i_T(t) = i_R(\boldsymbol{x}(t), v(t)) + C(\boldsymbol{x}(t), v(t))\frac{dv(t)}{dt} \quad (13)$$

$$\frac{d\boldsymbol{x}(t)}{dt} = f(\boldsymbol{x}(t), v(t)) \quad (14)$$

In this case $\boldsymbol{x}(t)$ is a state variable (or state vector if the state is defined by multiple variables) and i_R, C, and f represent continuous functions. In order to preserve zero-crossing behavior the following constraints may be required.

$$i_R(\boldsymbol{x}(t), 0) = 0 \quad (15)$$

$$C(\boldsymbol{x}(t), 0) = 0 \quad (16)$$

It is notable that it may be useful for ReRAM modeling to loosen the constraints of (15) and (16) under some cases by assuming equality with zero only under a limited range of the state variable. For example, in some forms of ReRAM such as TiO_2 resistance switching the zero-crossing behavior is not observed in the initial state prior to a formation step (see Fig. 1a of [11]).

V. CONCLUSION

This paper has shown that it is possible to construct a pinched hysteresis loop using a linear resistor and a non-linear capacitor. It is possible that at least some observations of pinched hysteresis

Lissajous curves may be indicative of square law capacitance or oscillation between positive and negative capacitance rather than a memristive effect. In cases where a memory effect is involved a more generic dynamic systems model has been proposed.

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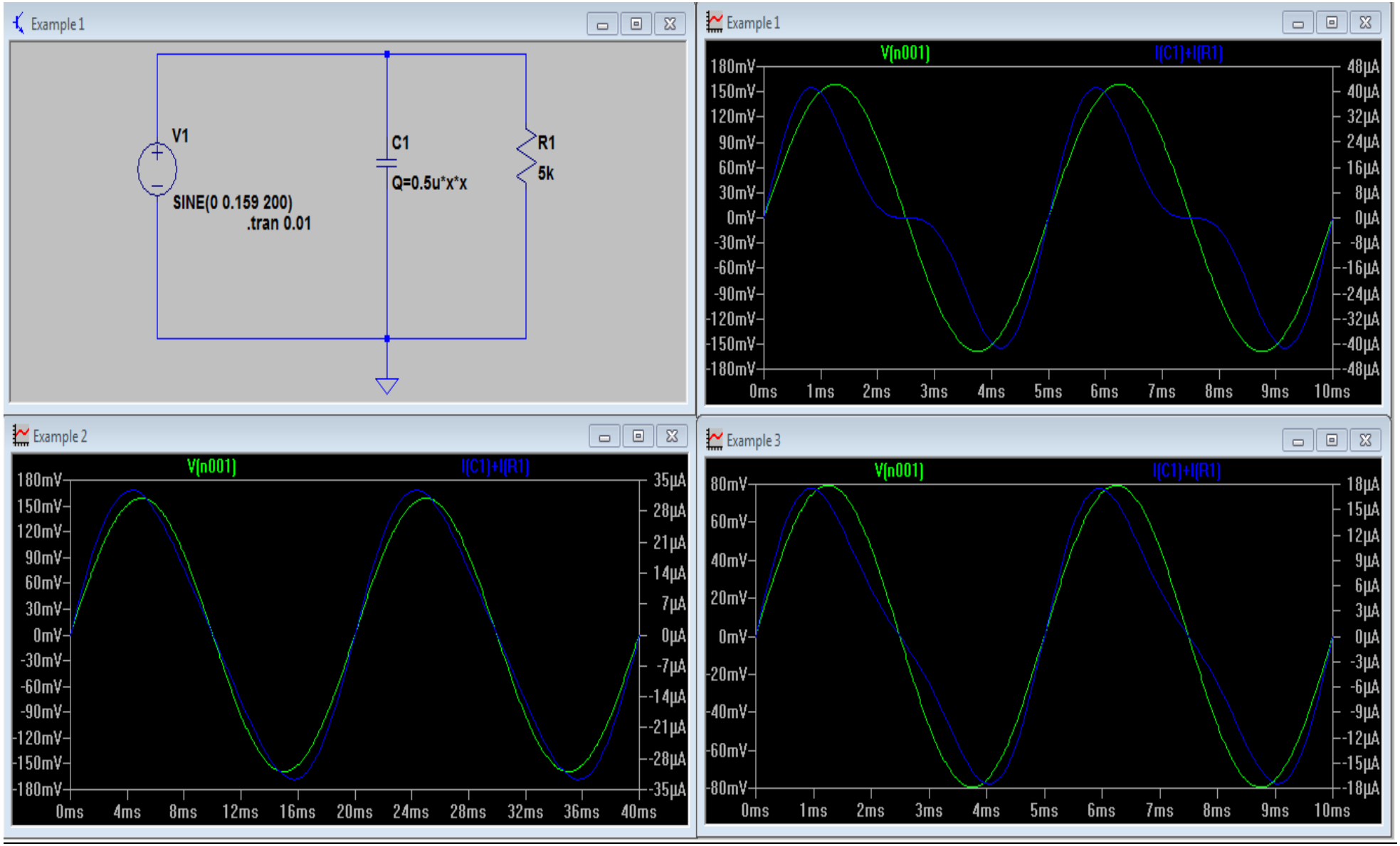
Example 1
V1
C1
R1
5k
Q=0.5u*x*x
SINE(0 0.159 200)
.tran 0.01
Example 1
V(n001)
I(C1)+I(R1)
180mV
150mV
120mV
90mV
60mV
30mV
0mV
-30mV
-60mV
-90mV
-120mV
-150mV
-180mV
48µA
40µA
32µA
24µA
16µA
8µA
0µA
-8µA
-16µA
-24µA
-32µA
-40µA
-48µA
0ms
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms
Example 2
V(n001)
I(C1)+I(R1)
180mV
150mV
120mV
90mV
60mV
30mV
0mV
-30mV
-60mV
-90mV
-120mV
-150mV
-180mV
35µA
28µA
21µA
14µA
7µA
0µA
-7µA
-14µA
-21µA
-28µA
-35µA
0ms
4ms
8ms
12ms
16ms
20ms
24ms
28ms
32ms
36ms
40ms
Example 3
V(n001)
I(C1)+I(R1)
80mV
60mV
40mV
20mV
0mV
-20mV
-40mV
-60mV
-80mV
18µA
15µA
12µA
9µA
6µA
3µA
0µA
-3µA
-6µA
-9µA
-12µA
-15µA
-18µA
0ms
1ms
2ms
3ms
4ms
5ms
6ms
7ms
8ms
9ms
10ms