DESIGN OF HIGH SPEED 64 BITS MULTIPLIER BY SQUARE FUNCTION

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Abstract. This article propose a new Booth multiplier design that the booth expansion is rearranged in square term like:

$$ab = ((a+b)^2 - a^2 - b^2)/2$$

If the code length of a, b is n, the multiplier on the right is with the size 2^{2n}, but multiplier on the left is with the size 2^n.

1. Introduction

The well-know design of booth multiplier is popularly used by core CPU. It's an algorithm like:

$$A = \sum_i a_i 2^{iN}, B = \sum_i b_i 2^{iN}, a_i, b_i < 2^N$$

$$AB = \sum_{i,j} a_i bj 2^{(i+j)N}$$

The efficiency of the designed is in fact decided by the next design of adders. Unavoidable the adders is of multi-levels. The least number of levels means of least time of delays of transistors and is more favorable.

2. Two level adder and three level adder

A high speed adder is so called *booth adder*, too, with the algorithm

$$A = \sum_{i=1}^{n} a_i 2^{iN}, B = \sum_i b_i 2^{iN}, a_i, b_i < 2^N$$

$$A + B = \sum_i S_i 2^{iN} + C_i 2^{(i+1)N} = S + C$$

$$S_i < 2^N, a_i + b_i = S_i \bmod 2^N$$

C_i is the carry of the addition of $a_i + b_i$. Despite of the long code of S, C the logics of $S + C$ is very simple with a design of size 2^{n+1} in one logical level.

In fact one can add three numbers in one stream like the algorithm of two number above

$$A = \sum_{i=1}^{n} a_i 2^{iN}, B = \sum_i b_i 2^{iN}, D = \sum_i d_i 2^{iN}, a_i, b_i, d_i < 2^N$$

$$A + B + D = \sum_i S_i 2^{iN} + C_i 2^{(i+1)N} = S + C$$

$$S_i < 2^N, a_i + b_i + d_i = S_i \bmod 2^N$$

The carry C_i ought to be $(00, 01, 10)_2$. The logical size of one bit of $S + C$ is of 3^{n+1} at most (this can be verified by simple analysis of the logics).

If one add four numbers at one stream like the above one can find the logical size of $S + C$ is 4^{n+1} approximately. The increasing numbers in a stream means that number increases very fast. So that three or four number add in one stream is favorable.

One has another choice solving addition of more numbers in 3-levels. It's feasible to separate the carries to two parts and process the addition in successive levels.

Two linked adders can solve relatively more numbers adding in one stream, but it must be concerned that more numbers means the less size of booths in order to district the size of designed circuits, and the carries must not disturb each others, or, the case is troublesome.

3. 64 bits multiplier design

Now I simply narrate the algorithm of my design:

- Separate the original multiplied to two 32-bits parts:

$$A = a_0 + a_1 2^{32}, B = b_0 + b_1 2^{32}$$

$$AB = a_0 b_0 + a_0 b_1 2^{32} + b_0 a_1 2^{32} + a_1 b_1 2^{64}$$

  The term $a_0 b_0$ is discarded.

$$AB = a_0 b_1 2^{32} + b_0 a_1 2^{32} + a_1 b_1 2^{64}$$

  Calculate in this order. The booth size of the adder is 7 and 5 bits if the addition is solved in two levels with relative larger size of circuits (approximately 20000 transistors) and cutting of trivial digits. It's also can be solved in less size by a three levels adder.
- Set

$$a_i b_j = ((a_i + b_j)^2 - a_i^2 - b_j^2)/2$$

  calculate in this order.
- Separate the $a_i, b_j, a_i + b_j$ to three 11-bits parts

$$a_i = A_0 + A_1 2^{11} + A_2 2^{22}$$

$$a_i^2 = (A_0 + A_1 2^{11} + A_2 2^{22})^2$$

$$= A_0^2 + A_1^2 2^{22} + A_2^2 2^{44} + 2A_0 A_1 2^{11} + 2A_0 A_2 2^{22} + A_1 A_2 2^{33}$$

$$= -A_0^2 + 2^{11}((A_0 + A_1)^2 - A_0^2 - A_1^2) + 2^{22}((A_0 + A_2)^2 - A_0^2 - A_2^2)$$

$$+2^{33}((A_1 + A_2)^2 - A_1^2 - A_2^2) + A_2^2 2^{44}$$

  A one level square function machine for 11-bit number is economic. The first step of calculation of this is addition of four number at most. This formula can be solved by four levels: one adder and a multiplier, successively two adders. In adders the booth size is suitably among $3, 4, 5, 7$.

4. CONCLUSION

According to the design above one can solve the 64-bit multiplier at approximately 23 levels (with larger size of circuits) or 24 levels (with less size of circuits) of delays of transistors like the explained in this article.

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